An Algorithm for Optimal Sizing of the Capacitor Banks under Non-sinusoidal and Unbalanced Conditions

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Abstract: In non-sinusoidal and unbalanced systems, optimal sizing of the capacitor banks is not a straightforward task as in sinusoidal and balanced systems. In this paper, by means of qualitative and quantitative analysis, it is interpreted that the classical capacitor selection algorithm widely implemented in Reactive Power Control (RPC) relays does not achieve optimal power factor improvement in non-sinusoidal and unbalanced systems. Accordingly, a computationally efficient algorithm is proposed to find the optimal capacitor bank for smart RPC relays. It is further shown in a simulated test case by using Matlab software that the proposed algorithm provides better power factor improvement when compared with the classical algorithm. It is also figured out from the simulation results that both algorithms cause almost the same harmonic distortion and unbalance deterioration levels in the system.
Keywords: Unbalanced conditions, nonsinusoidal conditions, power quality, power systems harmonics.

Short Running Title: Optimal Sizing of Capacitor banks in distorted environment

1. INTRODUCTION

In sinusoidal and balanced systems, conventional power resolution ($S^2=P^2+Q^2$) has been effectively utilized to measure the power transfer efficiency or power factor (pf=P/S) without any reservations by electrical engineering community [1]. Thus, it is well known for sinusoidal and balanced systems that the power of the compensation capacitor banks, which adjust power factor to near unity, is equal to the reactive-power (Q) measured at the load terminal, especially if the variation of the terminal voltage is negligible via compensation [2]. As a result, in sinusoidal and balanced systems, RPC relays have been employed to control the switched capacitors for the proper reactive-power compensation of the loads with variable power. In the present day's power systems, voltages and currents are non-sinusoidal and unbalanced due to the fact that large proliferation of non-linear and single-phase loads. For such systems, optimal capacitor sizing is not a straightforward process, as done for the sinusoidal and balanced systems [3]. Due to this fact, RPC relays generally select the capacitor banks by assuming the system is balanced and free from the harmonic pollution [4]-[7]. With respect to the classical algorithm widely implemented in the current RPC relays [4]-[7], the power quantities given in (1) are calculated for fundamental frequency using measured one line-to-line voltage and one line current:

$$S_1 = \sqrt{3} U_{\ell\ell 1} I_{\ell 1},\ cos\ \varphi_1 = \frac{P_1}{S_1},\ Q_1 = \sqrt{S_1^2 - P_1^2} \qquad (1)$$

Thus, the nameplate power of the delta connected balanced capacitor banks, which are needed to improve actual displacement power factor to its desired value, is determined as follows, where φ_1 is the difference between the fundamental harmonic phase angles of the line-to-neutral point voltage and the measured line current:

$$Q_{C-R} = P_1 \left(tan\ \varphi_1^{actual} - tan\ \varphi_1^{desired} \right) \qquad (2)$$

so that

$$dpf^{\ actual} = cos\ \varphi_1^{actual} = P_1 / S_1^{actual},$$

$$dpf^{\ desired} = cos\ \varphi_1^{desired} = P_1 / S_1^{desired}.$$

Additionally, for non-sinusoidal and unbalanced systems, some algorithms on the optimal sizing of the capacitive compensator are studied in the literature [8] - [10]. In [8], optimal reactances of the compensation capacitors are analytically calculated by considering the current minimization approach where the variation of the terminal voltage is negligible via compensation. For the most of the practical operation in three-phase systems the capacitor banks are employed as a delta balanced connection of the identical capacitors. However, this case was not considered for the modeling of the compensator in the same study. In addition to that, it does not consider the requirements, which are defined to prevent the detrimental effects of the non-sinusoidal voltages on the capacitor banks in IEEE Standard 18-2002 [11]. On the other hand, in non-sinusoidal and balanced systems of which the terminal voltage's variation is not negligible via compensation, [9] found optimal capacitive compensator using an optimization technique according to the combination of three criteria: maximizing true power factor, minimizing line loss and maximizing

average power transfer efficiency. For the same system conditions considered in [9], optimization problem of the capacitive compensator is separately solved according to each one of these three criteria in the study [10]. Due to the fact that both studies are based on the optimization technique, they can practically not be implemented in RPC relays.

In this paper, for optimum power factor improvement under non-sinusoidal and unbalanced conditions, the shortage of the compensator sizing algorithm (classical algorithm), which is widely employed in current RPC relays, is figured out by qualitative and quantitative analysis in Section **2**. An alternative method on the sizing of the capacitor banks is suggested for the three-phase and three-line applications of smart RPC relays in Section **3**. Finally, in Section **4**, the proposed method and the classical algorithm are comparatively analyzed in a simulated non-sinusoidal and unbalanced system case.

2. Shortage of the Classical Compensator Sizing Algorithm

For sinusoidal conditions, a compensation capacitor's rated power, which is generally called as ''Nameplate Power'' in electrical engineering community, is calculated using its capacitive reactance (X_C), rated voltage (U_R) and rated line frequency (f_R) [2]:

$$Q_{C-R} = \frac{U_R^2}{X_C} = 2\pi f_R C U_R^2 = U_R I_R,\ I_R = 2\pi f_R C U_R \quad (3)$$

Regarding systems with rated sinusoidal voltage; the reactive power drawn by a capacitor is equal to its nameplate power and the reactive power measured at the load terminals gives the nameplate power of the optimum compensation capacitor which adjusts power factor to its maximum value (unity) in this kind of systems. However, in non-sinusoidal systems, it is not easy to determine the nameplate power of the capacitor banks achieving optimum power factor improvement as in sinusoidal systems. This matter can be interpreted in an exemplary single-phase case, which consists of the voltage source with *THDU* (total voltage harmonic distortion) measured as 15% and R-L impedance load. In the exemplary case, load voltage and load current wave shapes are plotted in Fig (**1**).

For the case during the variation of the nameplate power (Q_{C-R}) of the compensation capacitor, fundamental harmonic reactive-power ($Q_1 = U_1 I_1 \sin\varphi_1$) measured at the load terminal, true power factor, $pf = \sum_h U_h I_h \cos\varphi_h \Big/ \sqrt{\sum_h U_h^2 \sum_h I_h^2}$, and displacement power factor (*dpf*) are shown in Fig. (**2**).

It is seen from Fig. (**2**) that Q_1 measured for the system without compensation gives the nameplate power of the capacitor which improve *dpf* to its maximum (unity). However, it is also seen that pf_{max} and dpf_{max} are obtained by using the different nameplate powers of the capacitor (0.488 pu and 0.7 pu respectively). It means that classical

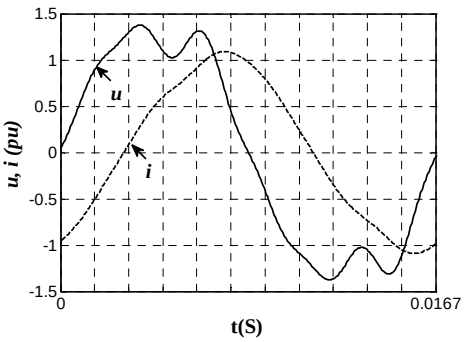

Fig. (**1**). The load voltage and load current in the exemplary case, *t* for time in seconds

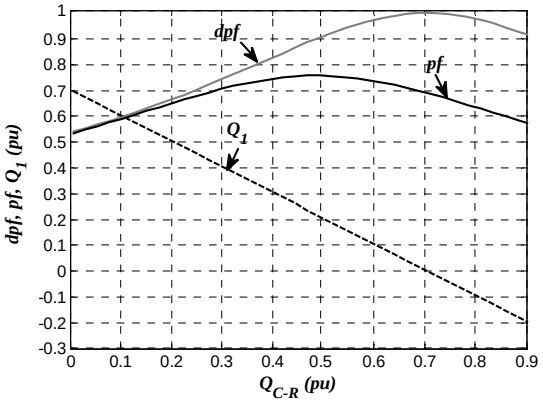

Fig. (**2**). Q_1, *dpf* and *pf* values measured at the load terminal during the variation of Q_{C-R}

method does not achieve pf_{max} in non-sinusoidal conditions. In addition to the above mentioned results, it is clearly understood from the literature [12]-[15] that there is no unique power factor definition for non-sinusoidal and unbalanced three-phase systems due to the fact that apparent power definition is still a discussion topic for this kind of systems. Furthermore, these studies also showed that IEEE Standard 1459-2010 [16] and DIN Standard 40110 [17] apparent power definitions can be employed for the effective measurement of power factor or power transfer efficiency.

First definition, apparent power defined in DIN Standard 40110, can be calculated for three-phase and three-line systems as;

$$S_\Sigma = U_\Sigma I_\Sigma = \sqrt{U_{a0}^2 + U_{b0}^2 + U_{c0}^2}\sqrt{I_a^2 + I_b^2 + I_c^2} \quad (4)$$

by using the rms values of phase currents (I_a, I_b, I_c) and the line-to-virtual star point voltages (U_{a0}, U_{b0}, U_{c0}) [12].

For three-phase and three-line systems, second definition, apparent power defined in IEEE Standard 1459-2010, is expressed as;

$$S_e = 3U_e I_e = 3\sqrt{\frac{U_{ab}^2 + U_{bc}^2 + U_{ca}^2}{9}}\sqrt{\frac{I_a^2 + I_b^2 + I_c^2}{3}} \quad (5)$$

When total line loss is written for three-phase and three-line systems with identical line resistances (r);

$$\Delta P = r\left(I_a^2 + I_b^2 + I_c^2\right) = rI_\Sigma^2 \quad (6)$$

It is obvious from (4), (5) and (6) that minimization of the total line loss can be obtained by maximizing power

factors calculated with respect to DIN Standard 40110 and IEEE Standard 1459-2010 definitions ($pf_{\Sigma} = P/S_{\Sigma}$ and $pf_{e} = P/S_{e}$) where voltage variation is negligible after the compensation. To achieve this goal, the balanced capacitor banks should minimize collective rms value of the line currents:

$$I_{\Sigma}^2 = I_a^2 + I_b^2 + I_c^2 = \frac{1}{T}\int_0^T \left(i_a^2 + i_b^2 + i_c^2\right)dt \tag{7}$$

However, classical method determines the nameplate power of the balanced capacitor banks regarding the fundamental harmonic reactive-power measured at one phase. Therefore, in three-phase and three-line systems with unbalanced and non-sinusoidal conditions, the current RPC relays can not maximize power factor encouraged by IEEE Standard 1459-2010 and DIN Standard 40110. Furthermore, they can cause lower or over compensation according to both standards.

3. PROPOSED ALGORITHM

The nameplate power of the optimal balanced capacitor bank, which maximizes true power factor encouraged by IEEE 1459-2010 and DIN 40110 standards, can be determined using the illustrative system given in Fig. (**3**).

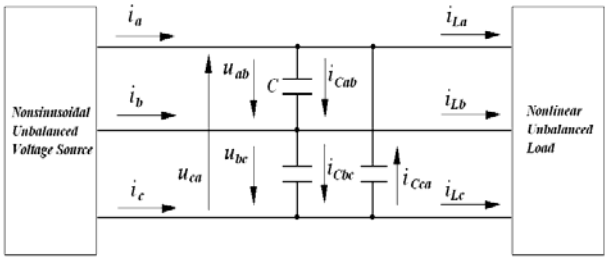

Fig. (**3**). An illustrative system used for the determination of the nameplate power of the optimal balanced capacitor bank

For the illustrative system, line-to-line voltages, load currents, compensator currents and line currents can be written as;

$$\begin{aligned} u_{ab} &= \sum_h \sqrt{2}U_{abh}\cos\left(h\omega t + \alpha_{abh}\right), \\ u_{bc} &= \sum_h \sqrt{2}U_{bch}\cos\left(h\omega t + \alpha_{bch}\right), \\ u_{ca} &= \sum_h \sqrt{2}U_{cah}\cos\left(h\omega t + \alpha_{cah}\right). \end{aligned} \tag{8}$$

$$\begin{aligned} i_{La} &= \sum_h \sqrt{2}I_{Lah}\cos\left(h\omega t + \beta_{Lah}\right), \\ i_{Lb} &= \sum_h \sqrt{2}I_{Lbh}\cos\left(h\omega t + \beta_{Lbh}\right), \\ i_{Lc} &= \sum_h \sqrt{2}I_{Lch}\cos\left(h\omega t + \beta_{Lch}\right). \end{aligned} \tag{9}$$

$$i_{Cab} = C\frac{du_{ab}}{dt},\quad i_{Cbc} = C\frac{du_{bc}}{dt},\quad i_{Cca} = C\frac{du_{ca}}{dt} \tag{10}$$

$$\begin{aligned} i_a &= i_{La} + C\frac{du_{ab}}{dt} - C\frac{du_{ca}}{dt}, \\ i_b &= i_{Lb} + C\frac{du_{bc}}{dt} - C\frac{du_{ab}}{dt}, \\ i_c &= i_{Lc} + C\frac{du_{ca}}{dt} - C\frac{du_{bc}}{dt}. \end{aligned} \tag{11}$$

By minimizing the collective rms value of the line currents with respect to the capacity,

$$\frac{d\left(I_{\Sigma}^2\right)}{dC} = \frac{d\left(I_a^2 + I_b^2 + I_c^2\right)}{dC} = 0 \tag{12}$$

the capacity of the capacitors placed in the optimum balanced compensator is found to be;

$$C_{opt} = \frac{1}{2\pi f_R}\cdot\frac{A}{2\left(B - D\right)} \tag{13}$$

where: A, B and D are expressed as;

$$\begin{aligned} A = &\sum_h hU_{abh}\begin{pmatrix} I_{Lah}\sin\left(\alpha_{abh} - \beta_{Lah}\right) \\ -I_{Lbh}\sin\left(\alpha_{abh} - \beta_{Lbh}\right)\end{pmatrix} \\ &+\sum_h hU_{bch}\begin{pmatrix} I_{Lbh}\sin\left(\alpha_{bch} - \beta_{Lbh}\right) \\ -I_{Lch}\sin\left(\alpha_{bch} - \beta_{Lch}\right)\end{pmatrix} \\ &+\sum_h hU_{cah}\begin{pmatrix} I_{Lch}\sin\left(\alpha_{cah} - \beta_{Lch}\right) \\ -I_{Lah}\sin\left(\alpha_{cah} - \beta_{Lah}\right)\end{pmatrix} \end{aligned} \tag{14}$$

$$B = \sum_h h^2U_{abh}^2 + \sum_h h^2U_{bch}^2 + \sum_h h^2U_{cah}^2 \tag{15}$$

$$\begin{aligned} D = &\sum_h h^2U_{abh}U_{cah}\cos\left(\alpha_{abh} - \alpha_{cah}\right) \\ &+\sum_h h^2U_{bch}U_{abh}\cos\left(\alpha_{bch} - \alpha_{abh}\right) \\ &+\sum_h h^2U_{cah}U_{bch}\cos\left(\alpha_{cah} - \alpha_{bch}\right) \end{aligned} \tag{16}$$

The nameplate power of the optimal balanced capacitor bank, which minimizes I_{Σ} and maximizes pf_{Σ} or pf_e, is found by substituting C_{opt} calculated from (13) in (17):

$$Q_{C-R} = 3\frac{U_{\ell\ell R}^2}{X_{Copt}},\ X_{Copt} = \frac{1}{2\pi f_R C_{opt}} \tag{17}$$

where $U_{\ell\ell R}$ is the rated line-to-line voltage of the capacitor bank.

Finally, the total rms values of each capacitor's current and total reactive powers drawn by each capacitors can be written as in (18) and (19):

$$\begin{aligned} I_{Cab} &= \frac{1}{X_{Copt}}\sqrt{\sum_h h^2U_{abh}^2}, \\ I_{Cbc} &= \frac{1}{X_{Copt}}\sqrt{\sum_h h^2U_{bch}^2}, \\ I_{Cca} &= \frac{1}{X_{Copt}}\sqrt{\sum_h h^2U_{cah}^2} \end{aligned} \tag{18}$$

$$Q_{Cab} = U_{ab}I_{Cab},\ Q_{Cbc} = U_{bc}I_{Cbc},\ Q_{Cca} = U_{ca}I_{Cca} \tag{19}$$

On the other hand, to prevent the detrimental effects of the non-sinusoidal voltages on the capacitors, the

following requirements included in IEEE Standard 18-2002 should be satisfied.

(i) The total rms currents (I_{Cab}, I_{Cbc}, I_{Cca}), which are calculated for each identical capacitors of the optimal compensator, should not exceed 135% of their rated current ($I_{C\text{-}R} = Q_{C-R}/(3U_{\ell\ell R})$).

(ii) The total rms value of the line-to-line voltages (U_{ab}, U_{bc}, U_{ca}) should not exceed 110% of the rated line-to-line voltage of the optimal compensator ($U_{\ell\ell R}$).

(iii) The total reactive powers (Q_{Cab}, Q_{Cbc}, Q_{Cca}), which are drawn by the capacitors placed in the optimal compensator, should not exceed 135% of their rated power ($Q_{C\text{-}R}/3$).

These limits can be formulated as;

$$\frac{max(I_{Cab}, I_{Cbc}, I_{Cca})}{I_{C-R}} \le 1.35 \quad (20)$$

$$\frac{max(U_{ab}, U_{bc}, U_{ca})}{U_{\ell\ell R}} \le 1.1 \quad (21)$$

$$\frac{max(Q_{Cab}, Q_{Cbc}, Q_{Cca})}{(Q_{C-R}/3)} \le 1.35 \quad (22)$$

Therefore, a representative pseudo code written for the proposed algorithm is stated below:

Step 1: Measure line-to-line voltages and line currents.

Step 2: Find the harmonic spectrums of the measured voltages and currents via DFT (Discrete Fourier Transform).

Step 3: Determine the rated power (Q_{C-R}) of optimal balanced capacitor bank from (17).

Step 4: Insert balanced capacitor banks with the rated powers around Q_{C-R} into the system.

Step 5: Let the tested capacitor bank, which provides the maximum pf_{Σ} value and the requirements given in (20)-(22), connect to the system.

4. COMPARITIVE ANALYSIS

The power factor improvement performances of the alternative algorithm presented in Section **3** and classical algorithm are comparatively analyzed by simulating the illustrative system given in Fig. (**3**). The system consists of the line-to-line voltages and load currents, which are plotted in Fig. (**4a**) and (**4b**). It is shown from this figure that both line-to-line voltages and load currents are non-sinusoidal and unbalanced. In the system, *THDU* and (U_1/U_{1+}) values are 5.00% and 2.05%, respectively. $THDI_{a,b,c}$ values of the load currents are 34%, 22% and 28%, respectively. In addition, the I_1/I_{1+} value of the load currents is measured as 28.60%.

In the test system, firstly, the maximum power factor value realizable via a balanced capacitor bank is determined. It was shown in [12]-[15] that DIN Standard 40110 and IEEE Standard 1459-2010 apparent power definitions give the same results for the three-phase and three-line system such as the illustrative one.

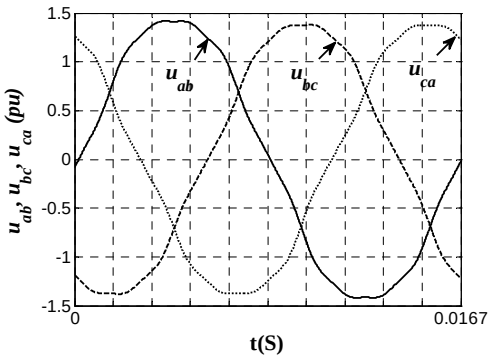

Fig. (**4a**). Line-to-line voltages

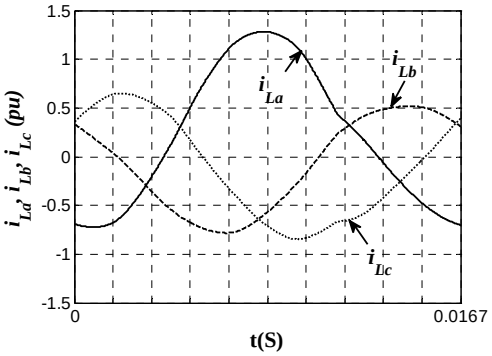

Fig. (**4b**). Load currents

Fig. (**4**). Line-to-line voltages and load currents

Thus, the variations of active power (*P*), one of apparent power definitions, DIN Standard 40110 apparent power (S_{Σ}), and power factor ($pf_{\Sigma}=P/S_{\Sigma}$) during increment of the nameplate power ($Q_{C\text{-}R}$) of the balanced capacitor bank are plotted in Fig. (**5**). Note that the nameplate power of the capacitor bank when power factor reaches its maximum ($pf_{\Sigma max}$) is pointed in the figure by a vertical line.

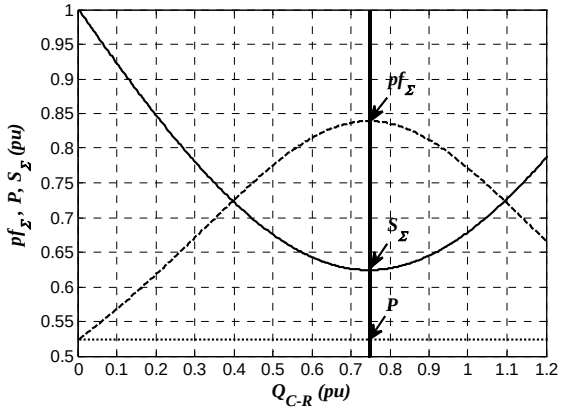

Fig. (**5**). The variations of active power and DIN Standard 40110 apparent power and power factor during the increment of the nameplate power of the balanced capacitor bank

It is shown from Fig. (**5**) that pf_{Σ} can be improved from 0.521 to 0.842 by means of the balanced capacitor bank. It is also carried out that $Q_{C\text{-}R}$ is 0.743 pu when pf_{Σ} reaches 0.842.

In the studied system, by using classical and proposed algorithms, the calculated $Q_{C\text{-}R}$ values and achieved pf_{Σ} levels are given in Table **I**. Classical method can be applied by implementing several voltage and current measurement strategies such as (i) measurement of u_{ab} and i_{Lc}, (ii) measurement of u_{bc} and i_{La}, and (iii) measurement of u_{ca} and i_{Lb}, are considered in the analysis. Thus, pf_{Σ} can be increased to 0.810, 0.757 or 0.830 using the balanced capacitor banks with the $Q_{C\text{-}R}$ values determined as 0.590, 1.028 or 0.785 pu respectively. One can see from the variation of pf_{Σ} with $Q_{C\text{-}R}$ plotted in Fig. (**5**) and Table **I** that the result of the classical algorithm depends on the measurement strategy and it can cause lower or over compensation with respect to IEEE Standard 1459-2010 and DIN Standard 40110.

On the other hand, pf_{Σ} attains 0.842 when the balanced capacitor banks, of which the nameplate power ($Q_{C\text{-}R}$) is determined as 0.743 pu according to proposed algorithm, is employed for the compensation.

In addition to the above mentioned results, I_1^-/I_1^+ and *THD* values of the line currents measured in the system compensated with respect to classical and proposed algorithms are given in Table **II**. This table shows that both algorithms cause almost the same deterioration in I_1^-/I_1^+ and *THD* values of the line currents. As a result, the proposed one does not have disadvantage on the deterioration in harmonic distortion and unbalance when compared with classical one. It should be noted that the deterioration in *THDI* can be reduced by means of passive filters [18]-[21].

TABLE **I**
CALCULATED NAMEPLATE POWERS OF THE BALANCED CAPACITOR BANKS AND ACHIEVED POWER FACTORS WITH RESPECT TO CLASSICAL AND PROPOSED ALGORITHMS

Methods	Measured voltage and current	$Q_{C\text{-}R}$ *(pu)*	pf_{Σ}
Classical Method	u_{ab}, i_{Lc}	0.590	0.810
	u_{bc}, i_{La}	1.028	0.757
	u_{ca}, i_{Lb}	0.785	0.830
Proposed Method	u_{ab}, u_{bc}, u_{ca} i_{La}, i_{Lb}, i_{Lc}	0.743	0.842

TABLE **II**
I_1^-/I_1^+ AND *THD* VALUES OF THE LINE CURRENTS FOR THE SYSTEM COMPENSATED WITH RESPECT TO CLASSICAL AND PROPOSED ALGORITHMS

Methods	THD_{Ia}	THD_{Ib}	THD_{Ic}	I_1^-/I_1^+
	All are given in percent (%)			
Classical Method	60	74	42	47
	82	78	43	45
	70	94	44	50
Proposed Method	64	90	41	49

5. CONCLUSIONS

At present day, the capacitor banks switched on and off automatically via RPC relays are still the most economical way for the reactive power compensation. However, in current RPC relays, the nameplate power of the capacitor banks is generally determined by assuming the system is balanced and free from the harmonic pollution. Due to this fact, current RPC relays are not adequate to maximize true power factor definition, which is encouraged by IEEE Standard 1459-2010 and DIN Standard 40110.

Consequently, under unbalanced and non-sinusoidal conditions, a computationally efficient algorithm is proposed to calculate the nameplate power of the optimal balanced capacitor bank, which maximizes the power factor definition of both standards, for implementation in smart RPC relays. It is seen from the results obtained in a simulated test case that the proposed algorithm provide better power factor improvement performance when compared with the classical algorithm.

CURRENT & FUTURE DEVELOPMENTS:

The shortage of the capacitor sizing algorithm (classical algorithm), which is widely employed in current RPC relays, is discussed under non-sinusoidal and unbalanced systems. It is further shown in a simulated unbalanced and non-sinusoidal test case that the proposed algorithm, which can practically be implemented in the smart RPC relays, provides better results on power factor improvement when compared with the classical algorithm.

The recent trend of harmonic system standards is considering the random nature of voltage and current harmonics. The IEC 1000-3-6 [22] uses probabilistic approaches both in comparing the actual current and voltage harmonic levels for distorting loads; the IEEE Standard 519 [23] slightly addresses the probabilistic application of harmonic distortion limits, but various efforts are in progress to more extensively include the probabilistic aspects. Consequently, the whole design basis may be redefined to include probabilistic aspects.

CONFLICT OF INTEREST:

The authors declare no conflict of interest.

NOMENCLATURE

$U_{\ell\ell 1}$: Fundamental harmonic line-to-line voltage,

$I_{\ell 1}$: Fundamental harmonic line current,

P_1 , Q_1 , S_1 : Fundamental harmonic active, reactive and apparent powers,

φ_1 : Difference between phase angles of fundamental harmonic line-to-neutral voltage and line current,

dpf: Displacement power factor,

u_{ab} , u_{bc} , u_{ca} : Instantaneous line-to-line voltages,

U_{ab} , U_{bc} , U_{ca} : Total rms values of the line-to-line voltages,

U_{abh} , U_{bch} , U_{cah} : Rms values of the *hth* harmonic line-to-line voltages,

α_{abh} , α_{bch} , α_{cah} : Phase angles of the *hth* harmonic line-to-line voltages,

I_{Lah} , I_{Lbh} , I_{Lch} : Rms values of the *hth* harmonic load current,

β_{Lah} , β_{Lah} , β_{Lah} : Phase angles of the *hth* harmonic load current,

i_a , i_b , i_c : Instantaneous line currents,

I_a , I_b , I_c : Total rms values of the line currents,

Q_{C-R} : Rated or nameplate power of the compensation capacitor,

S_Σ , U_Σ , I_Σ : Collective apparent power, collective rms voltage and collective rms current defined in DIN Standard 40110, respectively,

S_e , U_e , I_e : Equivalent apparent power, equivalent rms voltage and equivalent rms current defined in IEEE Standard 1459-2010, respectively,

pf_Σ , pf_e: Power factors calculated by considering DIN Standard 40110 and IEEE Standard 1459-2010 apparent power definitions.

THDU: Total harmonic distortions of the line-to-line voltages.

$THDI_a$, $THDI_c$, $THDI_c$,: Total harmonic distortions of a, b, c line currents.

U_1/U_{1+}: Ratio between magnitudes of the fundamental frequency negative- and positive- sequence voltages.

I_1/I_{1+}: Ratio between magnitudes of the fundamental frequency negative- and positive- sequence currents.

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