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Investigation of diode parameters using *I–V* and *C–V* characteristics of Al/maleic anhydride (MA)/p-Si structure

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Abstract. Al/maleic anhydride (MA)/p-Si metal–polymer–semiconductor (MPS) structures were prepared on p-Si substrate by spin coating. Device parameters of Al/MA/p-Si structure have been determined by means of capacitance–voltage (*C–V*) and conductance–voltage (*G–V*) measurements between 700 kHz and 1·5 MHz and current–voltage (*I–V*) measurements at 300 K. The parameters of diode such as the ideality factor, series resistance, barrier height (BH) and flat band barrier height were calculated from the forward bias *I–V* characteristics. The investigation of interface states that density and series resistance from *C–V* and *G–V* characteristics in Al/MA/p-Si device has been reported. The frequency dependence of the capacitance could be attributed to trapping states. Several important device parameters such as the BH ϕ_b, fermi energy (E_F), diffusion voltage (V_D), donor carrier concentration (N_D) and space charge layer width (W_D) for the device have been obtained between 700 kHz and 1·5 MHz. The *I–V*, *C–V-f* and *G–V-f* characteristics confirm that the parameters like the BH, interface state density (D_{it}) and series resistance (R_s) of the diode are strongly dependent on the electrical parameters in the MPS structures.

Keywords. Schottky barrier; ideality factor; series resistance; interfaces; organic compounds; electrical properties.

1. Introduction

Recently, there has been a great interest in polymer microelectronic devices because of their promising applications such as organic light-emitting diodes (Tang 1986), photovoltaic cells (Burrougher and Bradley 1990), field-effect transistors (Kwon *et al* 2011) and optoelectronic devices (Forrest *et al* 1982; Kilicoglu *et al* 2007a, b; Rajesh *et al* 2007; Aydin and Yakuphanoglu 2008). Owing to their stability and barrier height (BH) enhancement properties, organic materials have been employed particularly in electronic devices (Norde 1979; Cheung and Cheung 1986; Gupta *et al* 1991; Kuo *et al* 1994; Aydin *et al* 2006a, b). It is believed that the organic/inorganic semiconductor Schottky barrier diodes are useful to increase the quality of devices fabricated using the semiconductor (Sze 1981).

Polymeric interfacial layer in metal–polymer–semiconductor (MPS) structures play an important role in determining the main characteristics of electrical and dielectric parameters of organic optoelectronic devices. The performance of a MPS structure depends on various factors such as the presence of the localized interface states at the metal/organic polymer interfacial layer and organic polymer/semiconductor interfacial layer, metal to semiconductor BH, n and R_s of MPS diodes. Interfacial polymer layer and R_s are very important parameters of a MPS diode because the total voltage is shared by interfacial layer, depletion layer and series resistance of the diode when a voltage is applied to this diode. The magnitude of this shared voltage depends on the thickness and structure of interfacial layer and series resistance (Norde 1979; Cheung and Cheung 1986). Thereby, the performance and reliability of these devices depend especially on both series resistance and interfacial layer quality. R_s should be taken into account for an accurate and reliable determination of the electrical characteristics.

Analysis of the current–voltage (*I–V*) characteristics of the metal/semiconductor structures based on thermionic emission (TE) mechanism have shown an increase of n particularly in the existence of organic interfacial layer (Forrest *et al* 1982, 1984; Antohe *et al* 1991; Gupta and Singh 2004; Aydin *et al* 2006a, b; Aydin and Turut 2007; Kilicoglu *et al* 2007a, b; Rajesh and Menon 2007). The capacitance–voltage (*C–V*) and conductance–voltage (*G–V*) measurements ensure major information not only on the interface between dielectric film and semiconductor (Torres and Taylor 2005; Wang *et al* 2006), for example, the density of states of interface traps, but also about the semiconductor layer, for example, bulk mobility and doping density (Torres and Taylor 2005). The states of interface traps generally cause a frequency dispersion and bias shift of the *C–V* and *G–V* plots (Werner 1989; Tung 1992). The frequency dependence of the capacitance can be referred to trapping centers of majority carriers and relaxation processes of

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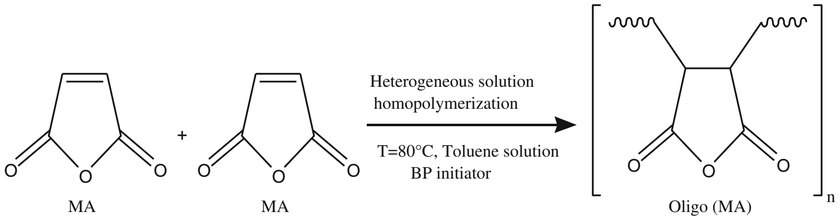

Figure 1. Synthetic route of oligo (MA).

these traps existing in the depleted region (Hasegawa and Abe 1982). Therefore, the frequency dependence of *C–V* and *G–V* plots are most important to obtain correct and trustworthy results.

Metal–semiconductor (MS) Schottky barrier diodes with an interfacial polymer such as polyaniline, poly(alkylthiophene), polypyrrole, polythiophene, poly(3-hexylthiophene) and polyvinyl alcohol (PVA) are taken into account as research topics because of their potential applications and interesting properties by chemists, physicists and electrical engineers as well (Bhajantri *et al* 2007; Gupta *et al* 2009). Any research has been found that maleic anhydride (MA) was used as interfacial polymers in literature. It is an excellent monomer and has reactive anhydride or hydrolyzed anhydride functional groups (carboxylic groups) (Zhou *et al* 2005). MA can be polymerized by various methods (Kahraman *et al* 2011) such as radical solution (Gaylord 1975; Trivedi and Culbertson 1982; Rzaev 1985), electrochemical (Bhadani and Saha 1980), plasma (Ryan *et al* 1996), UV (Tomescu and Macarie 1975) and γ-irradiation (Braun *et al* 1969), high pressure (Hamann 1967; Holmes-Walker and Weale 1955) and solid state (Babare *et al* 1967) polymerizations. Low-molecular-weight poly (MA) is called as oligo (MA) and known as biopolymer. Poly (MA) and their derivatives are widely used in industrial cooling water, boiler water, oil field injection, sugar mill evaporator, reverse osmosis, desalination and bioengineering applications (Babare *et al* 1967; Charles *et al* 1996). But, oligo (MA) derivatives have not been studied enough. Synthetic route of oligo (MA) is shown in figure 1, and the detailed information about the synthesis can be found in the article of Kahraman *et al* (2011).

In this paper, the spin coating technique was used to deposit MA on p-Si. To examine the effect of series resistance and interface states on *C* and *G* values, *C–V* and *G–V* measurements of the diode were performed at room temperature in the frequency range of 700 kHz–1·5 MHz. In addition, *C–V* and *G–V* characteristics of device were analyzed in detail to obtain some diode parameters.

2. Experimental

In this work, the samples were prepared on p-type Si(111) wafer which had 280 μm thickness and 10 Ω resistivity. Chemical cleaning procedures were applied before processing the wafer. Firstly, it was dipped into acetone for 10 min at 50 °C then washed by deionized water and released into methanol for 2 min. After methanol bath, the wafer was inserted in NOH_4:H_2O:H_2O_2 solution for 15 min at 70 °C. It was dipped into deionized water to remove solution on the wafer surface. In order to take away free oxygen on the surface, the wafer was bathed in 2% HF solution for 2 min. Finally, deionized water was used to complete the cleaning procedure. Following surface cleaning, aluminum (Al) metal with purity of 99·99% was thermally evaporated on the whole back surface of the wafer with thickness of 640 Å. Then, the wafer was annealed at 500 °C in vacuum for 10 min to dope aluminum into back surface of wafer. Again, the ohmic contact thickness of 800 Å was made by evaporating Al metal on the back of the p-Si substrate. Next, an MA organic film was formed by the spin coating technique. MA and dimethylformamide (DMF) were mixed in 2:1 molar ratio, and stirred for an hour. The film was deposited by spin coating at 500 rpm for 1 min and then at 1700 rpm for 45 s on polished surface of the wafer. Finally, rectifying contacts were deposited on organic film with a diameter of 1·3 mm using a metal shadow mask by evaporating 99·999% purity Al metal with thickness of 800 Å. All evaporation processes were carried out in a vacuum coating unit at about in 2×10^{-6} Torr placed inside the vacuum chamber. The *I–V* and *C–V* measurements were taken at room temperature for determining the electrical characteristics of the Schottky diodes. The schematic representation of the devices is shown in figure 2. The capacitance and conductance measurements were obtained between 700 kHz–1·5 MHz by using LF

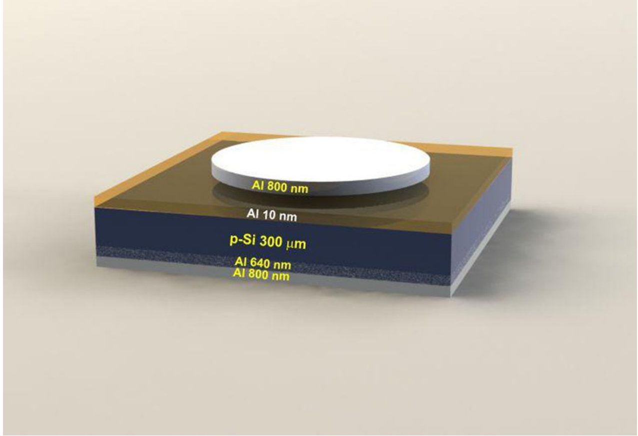

Figure 2. Schematic representation of the Al/MA/p-Si device.

impedance analyzer (HP4192A). The *I–V* measurements have been obtained using a 2410 Source Meter. All measurements were carried out at 300 K.

3. Results and discussion

3.1 *Current–voltage characteristics*

When the non-ideal Schottky diodes (MS) with a series resistance is considered, it is assumed that the net current of device is due to TE current and it can be given by the relations (Sze 1981; Rhoderick and Williams 1988)

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{1}$$

and

$$I_0 = AA^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right), \tag{2}$$

where I_0 is the saturation current derived from the straight line intercept of the ln *I–V* plot at $V = 0$, ϕ_b the effective barrier height at zero bias, A^* the Richardson constant and equals to 32 A/cm^2 K^2 for p-type Si, q the electron charge, V the applied voltage, A the diode area, k the Boltzmann constant, T the temperature in Kelvin and n the ideality factor. The experimental values of n and ϕ_b can be obtained from slopes and intercepts of the forward bias ln I vs voltage (V) plot, respectively, as

$$n = \frac{q}{kT}\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} \tag{3}$$

and

$$\phi_b = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right). \tag{4}$$

The forward and reverse bias measurements of the Al/MA/p-Si device were carried out at room temperature and are shown in figure 3. The values of n and ϕ_b were calculated from the forward semilog *I–V* characteristics using (3) and (4), respectively, and are given in table 1.

The Al/MA/p-Si device with a large value of n is far from ideal because of the presence of a polymer layer and the interface states. These values indicate that the current flow mechanism across the interface is also because of the generation–recombination and leakage currents. High values of n can be attributed to the presence of interfacial thin native oxide layer, to a wide distribution of low-Schottky barrier height (SBH) patches (or barrier in homogeneities) and to the bias voltage dependence of SBH (Kilicoglu *et al* 2007a, b). The corresponding values of n and SBH are 1·39 and 0·78 eV for Al/MA/p-Si device, respectively. Increasing of ϕ_b and n values have been attributed to particular distribution of interface states and polymeric composite layer between the metal and semiconductor. The underlying cause can be current mechanism of the structure, BH inhomogeneity, recombination–generation, series resistance and image-force lowering which is voltage dependent and/or an interfacial layer (Kilicoglu *et al* 2007a, b).

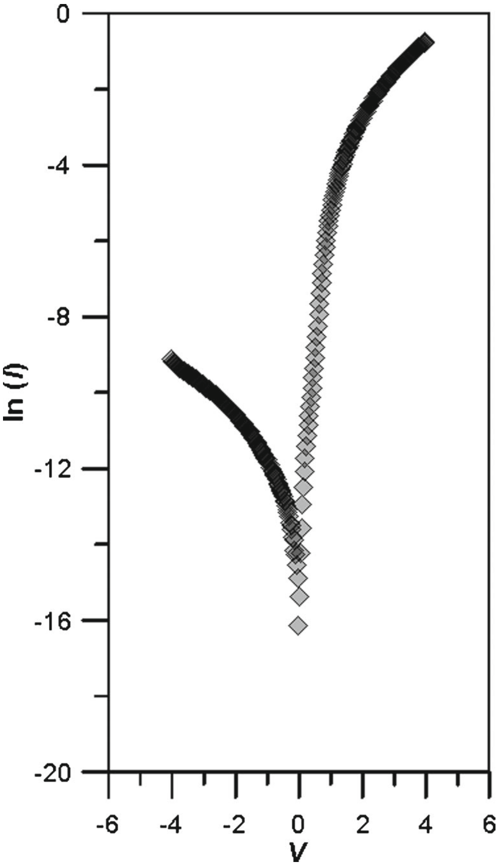

Figure 3. Experimental forward- and reverse-bias semi-logarithmic *I–V* characteristic of the Al/MA/p-Si Schottky barrier diode at room temperature.

Table 1. Electrical parameters from calculated *I–V* measurements of Al/MA/p-Si structures at room temperature in dark.

	$I-V$ parameters		
Methods	n	ϕ_b (eV)	R_s (Ω)
Standard	1·39	0·78	–
Cheung	1·98	0·82	27·2

R_s is an important paramater in the electrical characteristics of MPS diodes. This parameter is significant in the downward curvature of the forward bias *I–V* characteristics, but the other two parameters (n and ϕ_b) are significant in both the linear and non-linear regions of *I–V* characteristics. The values of R_s, n and ϕ_b were achieved using a method developed by Cheung and Cheung (1986). According to this method, the function can be written as

$$\frac{\mathrm{d}V}{\mathrm{d}(\ln I)} = n\frac{kT}{q} + IR_s, \tag{5}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^*T^2}\right) \tag{6}$$

and $H(I)$ is given

$$H(I) = n\phi_b + IR_s, \tag{7}$$

where ϕ_b is the BH obtained from data of the downward curvature region in the forward bias I–V characteristics.

In figure 4, experimental $dV/d(\ln I)$ vs I and $H(I)$ vs I plots are presented for the Al/MA/p-Si device at room temperature, respectively. Equation (5) should give a straight line for the data of the downward curvature region in the forward bias I–V characteristics. Where a plot of $dV/d(\ln I)$ vs I will be linear and gives R_s as the slope and nkT/q as the y-axis intercept. Using the n value determined from (5) and the data of the downward curvature region in the forward bias I–V characteristics in (6), a plot of $H(I)$ vs I will also lead to be a straight line (as shown in figure 4) with the y-axis intercept equal to $n\phi_b$. The slope of this plot also determines R_s which can be used to check the consistency of this approach. R_s, ϕ_b and n values for Al/MA/p-Si device are given in table 1. n and ϕ_b values obtained from (3) and R_s value obtained from (4) are found to be 1·10, 0·79 and 21 Ω for Al/p-Si structure, respectively. Values calculated for Al/p-Si structure are different from Al/MA/p-Si structure, which shows that the maleic layer has a significant effect on the BH of Al/MA/p-Si Schottky device and the maleic layer film appears to cause a significant modification on interface states. The difference between obtained ϕ_b values suggests that the barriers are non-uniform. The existence of layer between metal and semiconductor affects the properties of the interfacial layer. The BH is different from an ideal diode because of the potential drop across the interfacial layer (Gullu *et al* 2008a, b). The interface states may form either during the surface preparation or the evaporation of metal.

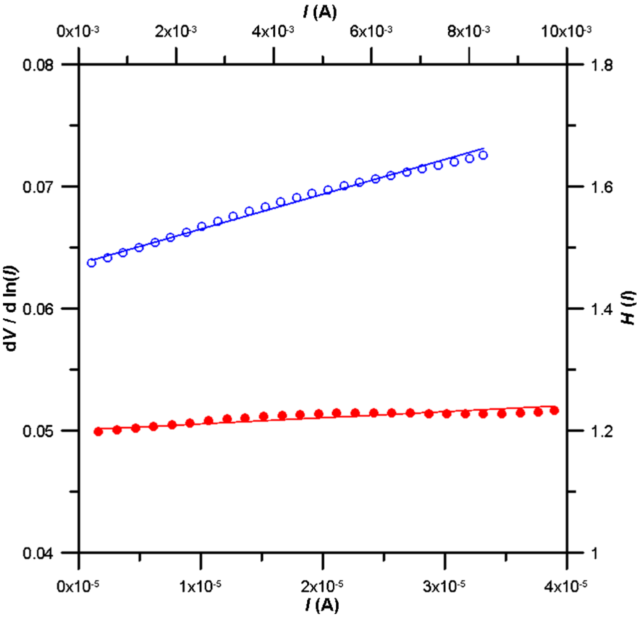

Figure 4. $dV/d(\ln I)$ vs I and $H(I)$ vs I characteristics of Al/MA/p-Si structure at room temperature in dark.

3.2 *Analysis of capacitance–voltage characteristic of Al/MA/p-Si diodes*

Figure 5(a) and (b) shows the C–V and G–V characteristics for Al/MA/p-Si device fabricated between 700 kHz and 1·5 MHz and at 300 K. The applied voltage range was taken between −4 and +4 V DC. According to figure 5(a) and (b), the device curves have accumulation, depletion and inversion regions for all the frequencies and dependent on voltage and frequency. The shape of the C–V curves for each frequency indicates p-type behaviour (Sze 1981). It is observed that the measured C and G are strongly dependent on bias voltage and frequency. As seen from figure 5(a) and (b), the values of capacitance and conductance increase with the decreasing frequency especially in the depletion region because of the existence of D_{it} and interfacial polymer layer. Effect of the interface state density can be eliminated when the C–V and G–V curves are measured at sufficiently high

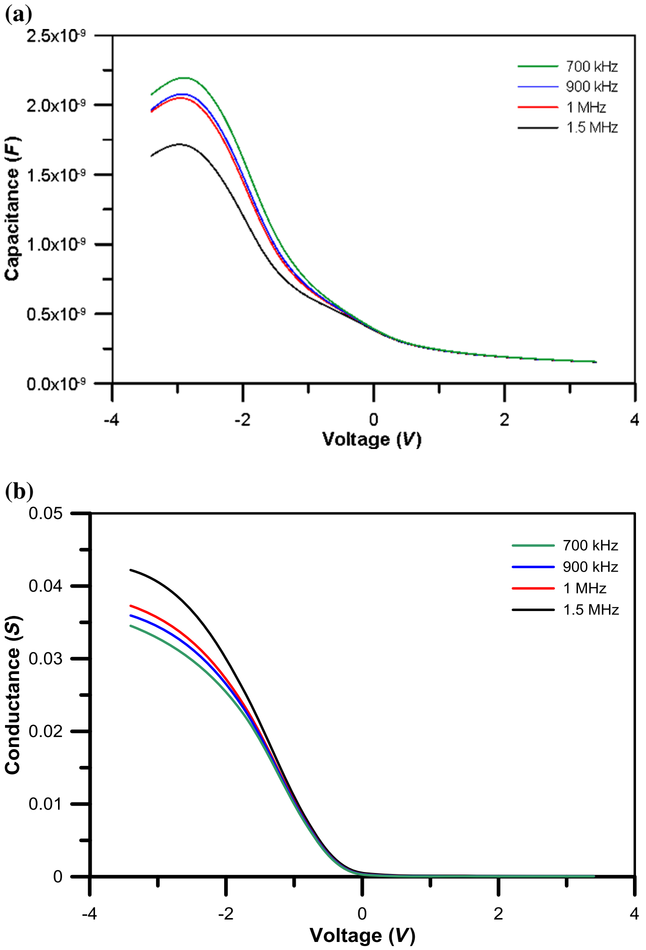

Figure 5. (**a**) Capacitance (C) and (**b**) conductance (G) characteristics vs voltage from 700 kHz to 1·5 MHz for Al/MA/p-Si device.

frequency ($f \geq 500$ kHz), because the charges at the interface states cannot follow an a.c. signal (Yuksel *et al* 2008). In this case, the interface states are in equilibrium with the semiconductor. Such behaviour of the C and G forward voltage is attributed to particular distribution of D_{it}, interfacial polymer layer and effect of R_{s}.

R_{s} is an important parameter which causes deviations in the ideal C–V and G–V characteristics of MPS structures. In order to determine voltage dependence of the R_{s} values, admittance method was given by Nicollian and Brews (1982). This method hepls in determining the R_{s} values in the whole measured range diode. According to this method, the real value of R_{s} at sufficiently high frequencies ($f \geq 500$ kHz) and in strong accumulation region corresponds to the value of R_{s} for metal–insulator–semiconductor (MIS) or metal–oxide–semiconductor (MOS) structures and can be subtracted from the measured C_{m} and G_{m} values as following (Nicollian and Goetzberger 1967).

$$R_{\text{s}} = \frac{G_{\text{m}}}{G_{\text{m}}^2 + \omega^2 C_{\text{m}}^2}, \tag{8}$$

where ω is the angular frequency, C_{m} and G_{m} represent the measured capacitance and conducance in the strong accumulation region. Figure 6 shows the voltage dependence of R_{s} for Al/MA/p-Si device between 700 kHz and 1·5 MHz. The R_{s}–V plot gives a distinguishable peak from about -1 to $-0{\cdot}5$ V. As seen in figure 6, R_{s} is independent of voltage at the accumulation region and positive bias. It is shown in figure 6 that the R_{s} values decrease by increasing frequency in the frequency range of 700 kHz–1·5 MHz, vary from 184 to 89 Ω. R_{s} must be considered in obtaining the voltage- and frequency-dependent characteristics of device. The magnitude of peak increases with the decreasing frequency and the peak position shifts towards negative bias region because of reordering and restructuring under the applied voltage effect at various frequencies (Bülbül and Zeyrek 2006).

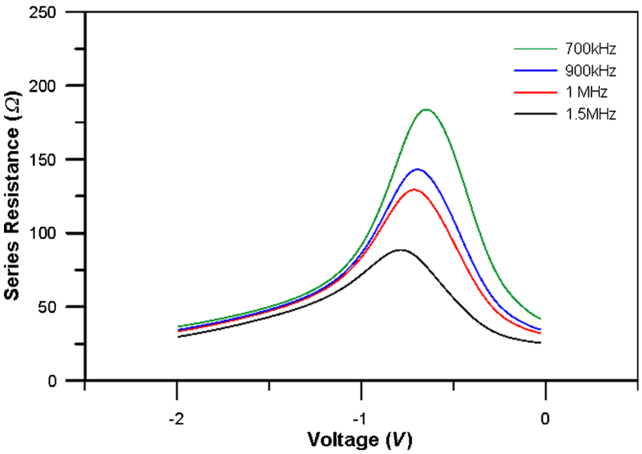

Figure 6. Determined R_{s}–V plots of the device at different frequencies.

In figure 7, the C^{-2}–V plot is presented for Al/MA/p-Si device between 700 kHz and 1·5 MHz. The C^{-2}–V plots of the MPS devices are linear for all frequencies in the depletion region. The slope corresponds to the localized doping concentration (Nicollian and Goetzberger 1967). This is derived from the standard Schottky–Mott analysis (Nicollian and Goetzberger 1967) where the doping concentration in a p-type semiconductor can be extracted in the depletion region via

$$\frac{\partial(1/C^2)}{\partial V} = \frac{2}{A^2 \varepsilon_{\text{s}} \varepsilon_0 q N_{\text{A}}}, \tag{9}$$

where C is the capacitance in the depletion region, A the area of device, V the gate voltage, N_{A} the ionized traps like acceptor which is determined from the slope of C^{-2}–V plot, ε_{s} the permittivity of the semiconductor ($\varepsilon_{\text{s}} = 11{\cdot}8\varepsilon_0$ for Si) and ε_0 the vacuum permittivity ($\varepsilon_0 = 8{\cdot}85 \times 10^{-12}$ F/m) (Rhoderick and Williams 1988). V_0 is the intercept of C^{-2} with the voltage axis and is given by

$$V_0 = V_{\text{d}} - kT/q. \tag{10}$$

Here, V_{d} is the diffusion potential at zero bias. The value of the BH $\phi_{\text{b}}(C-V)$ can be obtained by the relation

$$\phi_{\text{b}}(C-V) = V_{\text{d}} + E_{\text{F}} - \Delta\phi_{\text{b}}, \tag{11}$$

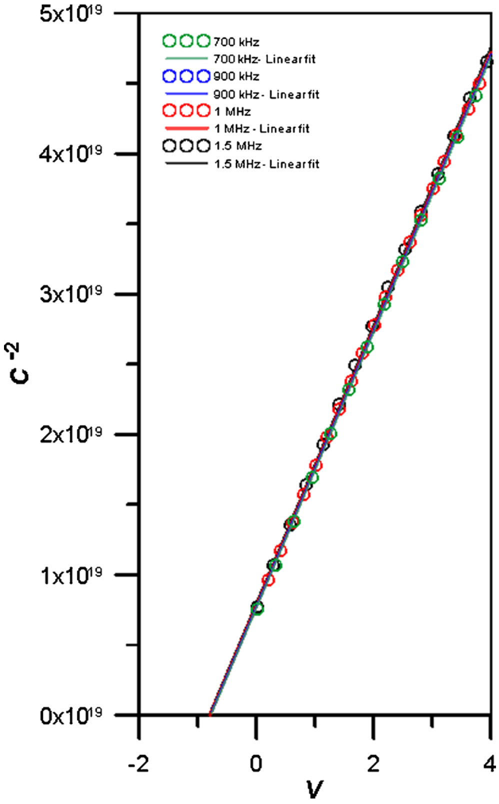

Figure 7. C^{-2}–V characteristics for the Al/MA/p-Si device between 700 kHz and 1·5 MHz.

where E_F is the energy difference between the bulk Fermi level and valance band edge, and is given by (Rhoderick and Williams 1988)

$$E_F = \frac{kT}{q} \ln\left(\frac{N_v}{N_A}\right) \tag{12}$$

with

$$N_v = 4{\cdot}82 \times 10^{15} T^{3/2} \left(\frac{m_h^*}{m_0}\right)^{3/2}, \tag{13}$$

where N_v is the effective density of states in Si valance band, m_h ($= 0{\cdot}16m_0$) is the effective mass of holes and m_0 is the rest mass of the electron. $\Delta\phi_b$ is the image force barrier lowering and is given by (Rhoderick and Williams 1988)

$$\Delta\phi_b = \left(\frac{qE_{max}}{4\pi\varepsilon_s\varepsilon_0}\right)^{1/2}, \tag{14}$$

where E_{max} is the maximum electric field and given by (Rhoderick and Williams 1988)

$$E_{max} = \frac{2qV_0N_A}{\varepsilon_s\varepsilon_0}. \tag{15}$$

The obtained values of E_F, V_0, N_A, $\Delta\phi_b$ and $\phi_b(C-V)$ are given in table 2. While the value of N_A almost linearly decreases, the value of $\phi_b(C-V)$ linearly increases with increasing frequency. Such behavior of N_A and $\phi_b(C-V)$ is an expected behavior and it is attributed to the particular density distribution of interface states and interfacial layer (Rhoderick and Williams 1988).

As seen from the obtained values, the difference between $\phi_b(I-V)$ and $\phi_b(C-V)$ for the Al/MA/p-Si diode originates from the difference in nature of both the I–V and C–V measurements. Due to different nature of the C–V and I–V measurement techniques, the barrier heights deduced from them are not always the same. The capacitance C is insensitive to potential fluctuations on a length scale of less than the space charge region and C–V method averages over the whole area and measures to describe BH. The DC current I across the interface depends exponentially on the BH and thus sensitively on the detailed distribution at the interface (Rhoderick and Williams 1988; Werner 1989). Additionally, the discrepancy between the BH values of the device may also be explained by the existence of the interfacial layer and the trap states in the semiconductor (Wagner *et al* 1983). Consequently, the BH values obtained from C^{-2}–V characteristics at various frequencies are remarkably higher than the values obtained from I–V characteristics at room temperature.

Table 2. Values of different device parameters for Al/MA/p-Si diode calculated from C_c–V and G_c–V characteristics between 700 kHz and 1·5 MHz.

Frequency	700 kHz	900 kHz	1 MHz	1·5 MHz
N_A ($\times 10^{16}$cm^{-3})	1·981	1·976	0·690	0·687
V_0 (V)	0·780	0·791	0·795	0·811
E_F (meV)	156·588	156·650	182·947	183·064
W_d ($\times 10^{-5}$.cm)	2·304	2·321	3·938	3·986
$\Delta\phi_b$ (meV)	29·191	29·267	22·527	22·611
ϕ_b (eV)	0·933	0·943	0·980	0·996
C_i (nF)	2·290	2·168	2·130	1·786
$G_{c,m}$ ($10^{-2}\times$S)	3·711	4·333	4·674	6·767
C_c (nF)	6·688	7·637	8·373	11·817
$R_s\Omega$	184	143	129	89
D_{it} ($\times 10^{11}$ eV^{-1}/cm^2)	4,60273	3,8272	3,370	1,417

The discrepancy can be due to the organic layer plus interfacial native oxide layer between the metal and the p-Si. In addition, the existence of BH inhomogeneity could be another explanation for this discrepancy (Aydin *et al* 2006a, b; Kilicoglu *et al* 2007a, b). The width of the depletion layer (W_d) has been determined as

$$W_d = \sqrt{\frac{2\varepsilon_s V_0}{qN_A}}. \tag{16}$$

In addition, frequency dependence of interface states densities was obtained using the Hill–Coleman method which is very useful in understanding the electrical properties of the interface (Nicollian and Goetzberger 1967). According to this method, the D_{it} values can be calculated by using the following:

$$D_{it} = \frac{2}{qA}\left(\frac{(G_{c,max}/\omega)}{(G_{c,max}/\omega C_i)^2 + (1 - C_c/C_i)^2}\right), \tag{17}$$

where A is the rectifier contact area, ω the angular frequency, $G_{c,max}$ related to the maximum in the corrected G–V curve, C_c the capacitance to $G_{c,max}$ and C_i the capacitance of interfacial layer (Nicollian and Goetzberger 1967). The value of C_i can be obtained from the C–V and G–V measurements in strong accumulation region at various high frequencies, using the relation (Nicollian and Goetzberger 1967)

$$C_i = C_m\left[1 + \frac{G_m^2}{(\omega C_m)^2}\right] = \frac{\varepsilon_i\varepsilon_0 A}{d}. \tag{18}$$

The D_{it} values calculated from (18) are given in table 2. As seen in figure 8, the D_{it} values of the MPS device increase with decreasing frequency. Consequently, as shown in figure 8, both the values of D_{it} and R_s were found to decrease with the increasing frequency. These behaviors of R_s especially can be attributed to the interfacial polymer layer and particular distribution of localized density of the interface states between polymer interfacial layer and semiconductor interface (Bohlin 1986). According to table 2, the D_{it} values of the Al/MA/p-Si device increase with decreasing frequency. For instance, the obtained D_{it} values for the MPS device are $4{\cdot}60273\times10^{11}$ and $1{\cdot}417\times10^{11}$ eV^{-1} cm^{-2} for 700 kHz and 1·5 MHz, respectively. The energy distribution of the interface states of the diode changes from $2{\cdot}44\times 10^{12}$ to $1{\cdot}24\times10^{13}$ eV^{-1}cm^{-2}. Gullu *et al* (2008a, b) found that the deposition of polymers onto the inorganic

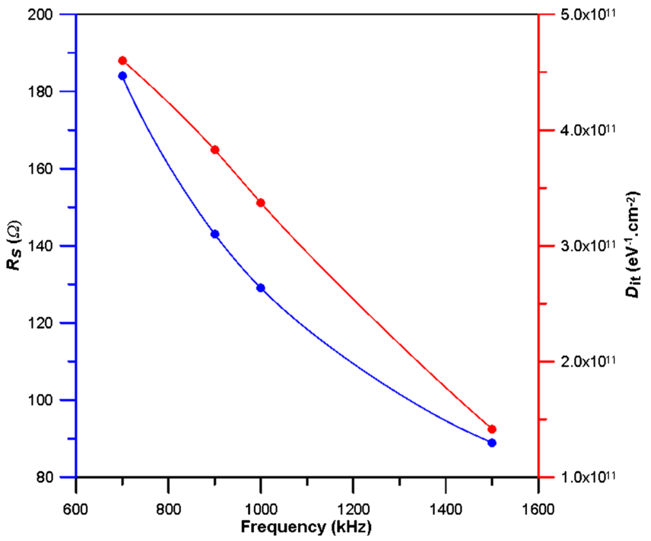

Figure 8. Variation in D_{it} and R_{s} as a function of frequency for the Al/MA/p-Si.

semiconductor could generate a large number of interface states at the semiconductor surface, which is strongly influenced by the properties of the PANI/p-Si/Al structure. Cakar *et al* (2007) have determined the interface properties of Au/PYR-B/p-Si/Al contact. They found that the interface state density values varied from $4{\cdot}21\times10^{13}$ to $3{\cdot}82\times10^{13}$ $\mathrm{eV^{-1}cm^{-2}}$. In another study, Aydin and Turut (2007) have investigated the interface state density properties of the Sn/methylred/p-Si/Al diode and the interface state density was found to vary from $1{\cdot}68\times10^{12}$ to $1{\cdot}80\times10^{12}$ $\mathrm{eV^{-1}cm^{-2}}$. It is evaluated that the interface properties of the Al/p-Si junction are changed depending on the organic layer inserted into the metal and semiconductor. The organic interlayer appears to cause a significant modification of interface states even though the organic–inorganic interface appears abrupt and unreactive (Yan *et al* 2006; Gullu *et al* 2008a, b). The MA organic layer increases the effective BH clearly upon the modification of the semiconductor surfaces and the chemical interaction at the interface of the MA organic layer to the p-Si and oxide–organic interface states will give rise to new interface states.

4. Conclusions

In summary, we have fabricated and investigated the electrical characteristics of the Al/MA/p-Si device formed by coating of the organic material to directly p-Si substrate. It has been seen that the MA thin film on p-Si substrate showed a good rectifying behaviour. The forward I–V characteristic of the device has been analyzed on the basis of the standard thermionic emission theory. The BH, ideality factor and series resistance of the device were calculated from the I–V characteristics and Cheung method.

The frequency-dependent capacitance–voltage (C–V-f) and conductance–voltage (G–V-f) characteristics of the metal–polymer–semiconductor (Al/MA/p-Si) were investigated between 700 kHz and 1·5 MHz at room temperature. The forward and reverse bias (C–V-f) and (G–V-f) characteristics of the MPS structure show that both capacitance and conductance are quite sensitive to frequency and voltage. Such a behavior of the C and G is attributed to particular distribution of interface states at the polymer interface and series resistance. Series resistance is dependent on both frequency and voltage and changes from accumulation to inversion. These behaviors considered that the trap charges have enough energy to escape from the traps at the metal–semiconductor interface in the Si band gap. The real series resistance of MPS structure can be obtained from the C–V and G–V measurements in strong accumulation regions at high frequencies. Interface states cannot follow ac signal in the accumulation region.

It is concluded from experimental results that the location of D_{it} between Si/MA and R_{s} has a significant effect on electrical characteristics of the Al/MA/p-Si device, which are responsible for the non-ideal behavior of the C–V characteristics. The developed Al/MA/p-Si MPS type can be used as a good electronic material combination for possible applications. This work declared here recommends that the MA interlayer should be considered, among other organics, as a potential thin film for the novel MPS devices.

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