




# Flipped Voltage Follower-Based Voltage Conveyors: Investigation and Possible Enhancements

Costas Psychalinos<sup>1</sup>  · Abdullah Yesil<sup>2</sup> · Shahram Minaei<sup>3</sup> · Panagiotis Bertisias<sup>1</sup>

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## Abstract

Second-generation voltage conveyor structures, based on the employment of flipped voltage follower stages, are investigated and proposed in this work. The proposed core has the feature of offering extremely low or electronically adjustable input resistance and programmable outputs, enhancing the achieved design flexibility and versatility of this active cell. Two design examples are presented in this work, including a multi-phase sinusoidal oscillator topology and an electronically adjustable first-order low-pass filter, both supported by simulation and experimental results.

**Keywords** Voltage conveyors · Flipped voltage follower · Multi-phase oscillators · Electronic tuning · Analog filters · Analog integrated circuits

## 1 Introduction

The second-generation voltage conveyors (VCIIs) are attractive alternatives of second-generation current conveyors (CCIIIs) and this is originated from the fact that they

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✉ Costas Psychalinos  
cpsychal@upatras.gr  
Abdullah Yesil  
ayesil@bandirma.edu.tr  
Shahram Minaei  
sminaei@dogus.edu.tr  
Panagiotis Bertisias  
panosber@upatras.gr

- 1 Electronics Laboratory, Physics Department, University of Patras, Rio Patras, Greece
- 2 Department of Electrical and Electronics Engineering, Bandirma Onyedi Eylul University, Balikesir, Turkey
- 3 Department of Electrical and Electronics Engineering, Dogus University, Umraniye, Istanbul, Turkey

offer a low-impedance output terminal, allowing their direct interconnection with other stages for implementing analog signal processing systems [21]. A significant number of such active cells have been already introduced in the literature, and they have been employed in several applications, including filters, capacitance multipliers, inductance emulators and oscillators [1–3, 13, 17, 18, 20, 22, 28, 29, 31, 34, 35]. One of the requirements that VCII must fulfill is the extremely low resistance at its terminals Y and Z. The topology in [29] offers such features with relatively low circuit complexity, but it suffers from the different dc levels at these terminals. There are also applications where external resistors could be substituted by the inherent (i.e., parasitic) resistance of the terminal Y, providing electronic adjustment capability of the derived structures, which is an attractive feature of nowadays systems. The VCII structures in [2, 17, 18] offer electronic adjustable parasitic impedance at node Y, but they suffer from the non-zero resistance at the output terminal Z and, also, from the increased circuit complexity. The VCII topology in [32] offers a relatively simple circuitry with electronically controlled resistance at node Y and an extremely low resistance at terminal Z, but the problem there is that the terminal Z is at a different dc level than that of the other terminals of VCII. A relatively simple VCII structure which offers extremely low resistances at both terminal Y and Z, without having different dc levels between these terminals, is presented in this work. An attractive feature of this topology is that it can be easily transposed into an electronically controllable structure, just by changing the point where the Y terminal is fed, providing design flexibility and versatility. This is achieved without losing the aforementioned features.

The paper is organized as follows: the basic structure is presented in Sect. 2, where possible enhancements for further increasing its usefulness are also provided. The performance of the proposed core is evaluated and compared with that of the already published relevant structures in Sect. 3 in order for the added value to be evident. A programmable multi-phase sinusoidal oscillator (MSO) topology and a first-order low-pass filter design are presented and evaluated in Sect. 4, as design examples.

## 2 Flipped Voltage Follower-Based Second-Generation Voltage Conveyors

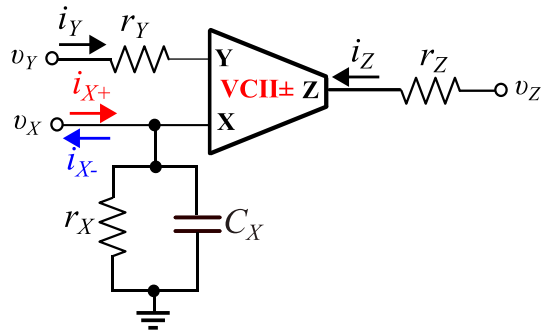
### 2.1 Proposed Topology of FVF-Based VCII

The symbol of a VCII is provided in Fig. 1, and the matrix equation which describes its behavior is the following:

$$\begin{bmatrix} i_X \\ v_Z \\ v_Y \end{bmatrix} = \begin{bmatrix} \pm\alpha & \frac{1}{r_X // C_X s} & 0 \\ 0 & \beta & r_Z \\ r_Y & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix}. \quad (1)$$

The current conveying operation in (1) between terminals Y and X is described by the factor  $+\alpha$  for a VCII+, and by the opposite one in the case of a VCII-; the factor  $\beta$  describes the voltage conveying operation between terminals X and Z. In addition,

**Fig. 1** Symbol of a VCII with the inherent resistance and capacitance at each terminal



$C_X$  are  $r_X$  are the inherent (parasitic) capacitance and resistance associated with the terminal X, and  $r_Y$ ,  $r_Z$  are the inherent resistances of terminals X and Z, respectively. For an ideal VCII, i.e.,  $\alpha = 1$ ,  $\beta = 1$ ,  $r_Y = 0$ ,  $r_X \rightarrow \infty$ ,  $r_Z = 0$ , and  $C_X = 0$ .

The FVF is an attractive stage for achieving the goal of the minimum input resistances at nodes Y and Z, and this is originated from the fact that the implemented resistances are scaled versions of the basic resistance  $1/g_m$ , with  $g_m$  being the transconductance parameter of a MOS transistor [4].

Such a topology with nMOS-pMOS conversion, introduced in [29], is depicted in Fig. 2.

Thanks to the employment of FVF in stages associated with the terminals Y and Z, the corresponding inherent resistances are

$$r_Y \simeq \frac{1}{g_{m,Mp1} (g_{m,Mp5} \cdot r_{0,Mp1})}, \quad (2)$$

$$r_Z \simeq \frac{1}{g_{m,Mp2} (g_{m,Mp7} \cdot r_{0,Mp2})}. \quad (3)$$

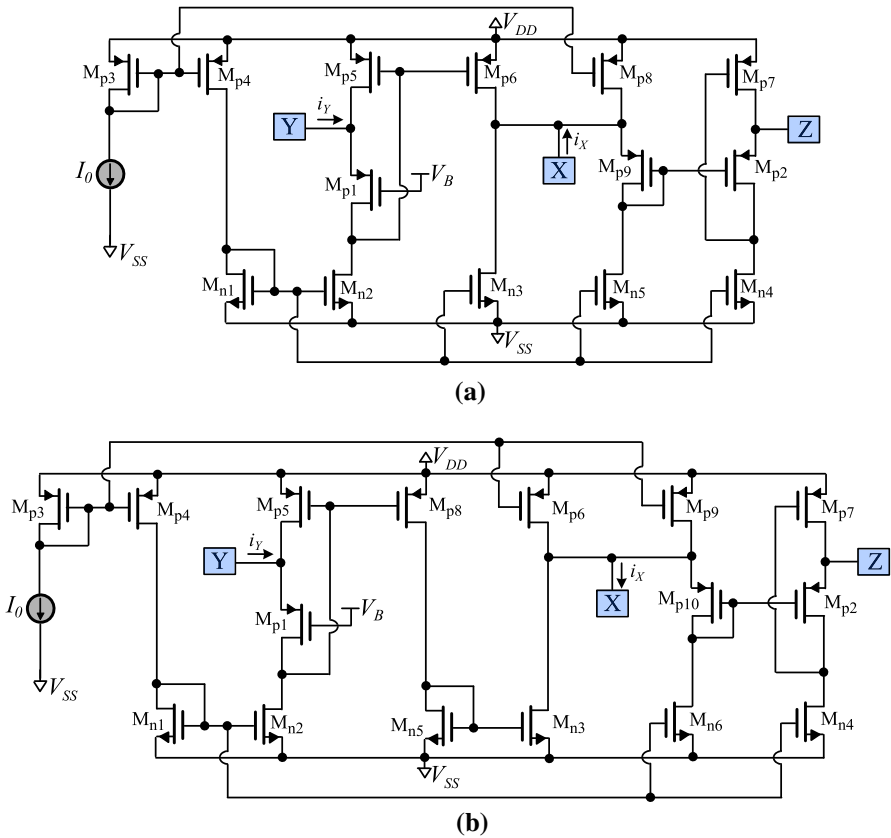
Inspecting (2)–(3), it is readily obtained that the “effective” transconductance seen from terminals Y and Z is scaled by a factor  $g_m r_0$ , and therefore, the corresponding input resistances are reduced by the same factor. This is a benefit with regard to the convectional way for implementing the required ac ground at terminal Y as well as the voltage conveying between terminals X and Z, where a differential-pair in cascade connection with a voltage follower have been employed, offering inherent resistances equal to  $1/g_m$  at these terminals. It must be pointed out that reduced values of  $1/g_m$  can be implemented by these stages, but the values of the dc bias currents of these stages must be significantly increased making the power dissipation of the active cell not reasonable for practical applications.

The inherent resistance at terminal X is:

$$r_X = r_{0,Mn3} / r_{0,Mp6}. \quad (4)$$

A practical problem that occurs in the topology of Fig. 2 is related to the dc levels of the terminals voltages. More specifically, the dc level at terminal Y is determined by the value of the extra dc supply voltage connected at the gate of Mp1, being equal to  $V_B$





**Fig. 3** Proposed modifications of the scheme in Fig. 2 for realizing **a** VCII+, and **b** VCII- with equalized dc operating point voltages at all terminals

scheme in Fig. 4a offers design modularity and versatility, in the sense that the same core can be used for realizing various types of transfer function.

The topologies in Fig. 3 can be fed at different point in order to take advantage of the electronic tuning capability of the small-signal transconductance parameter. This is demonstrated in Fig. 5a and, assuming operation of MOS transistors in the strong inversion region, the resistance associated with terminal Y is given by (5)

$$r_Y \simeq \frac{1}{g_{m,Mp5}} \tag{5}$$

Therefore, the resistance can be tuned through the corresponding dc bias current  $I_0$ , while the other inherent resistances are still given by (3)–(4). This circuit will be mentioned hereinafter as current-controlled VCII (CCVCII), in correspondence with the notation of a current-controlled second-generation current conveyor (CCCII), where the inherent resistance at node X is electronically controllable. The associated symbol of the CCVCII is depicted in Fig. 5b.

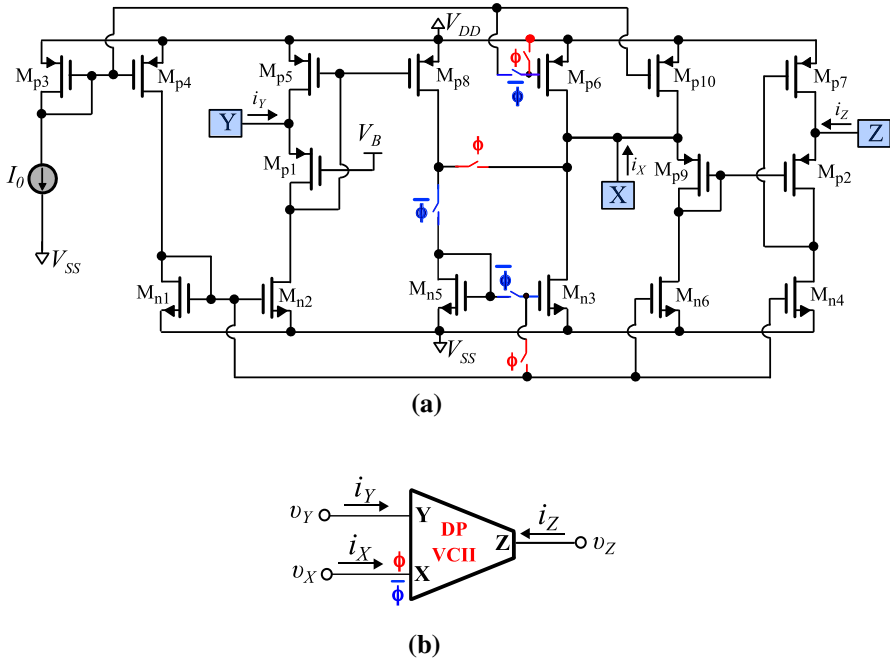


Fig. 4 Digitally programmable VCIH (DP-VCIH) with dual output capability **a** circuitry, and **b** its associated symbol

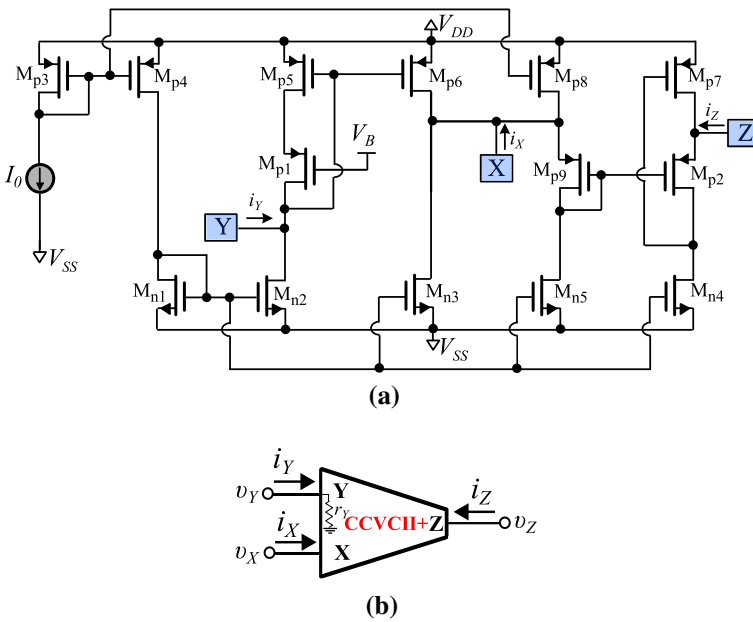
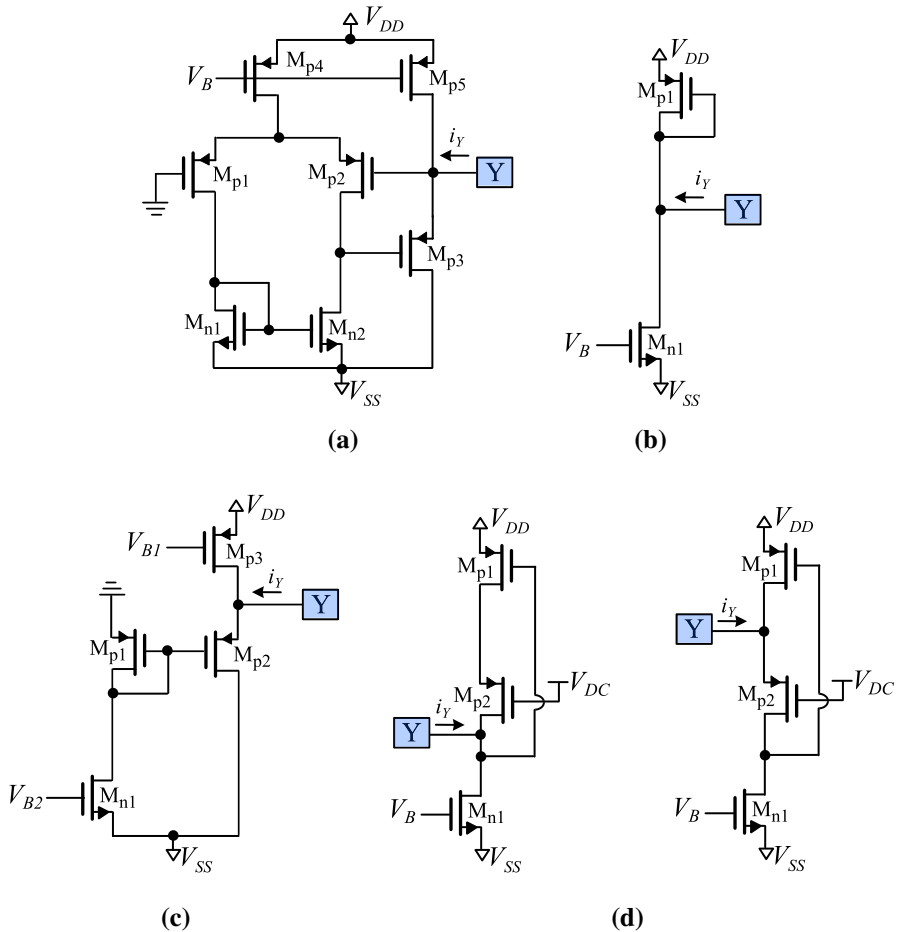


Fig. 5 Current-controlled VCIH (CCVCIH) **a** circuitry , and **b** its associated symbol



**Fig. 6** Possible implementations of the input stage related on terminal Y of a VCII

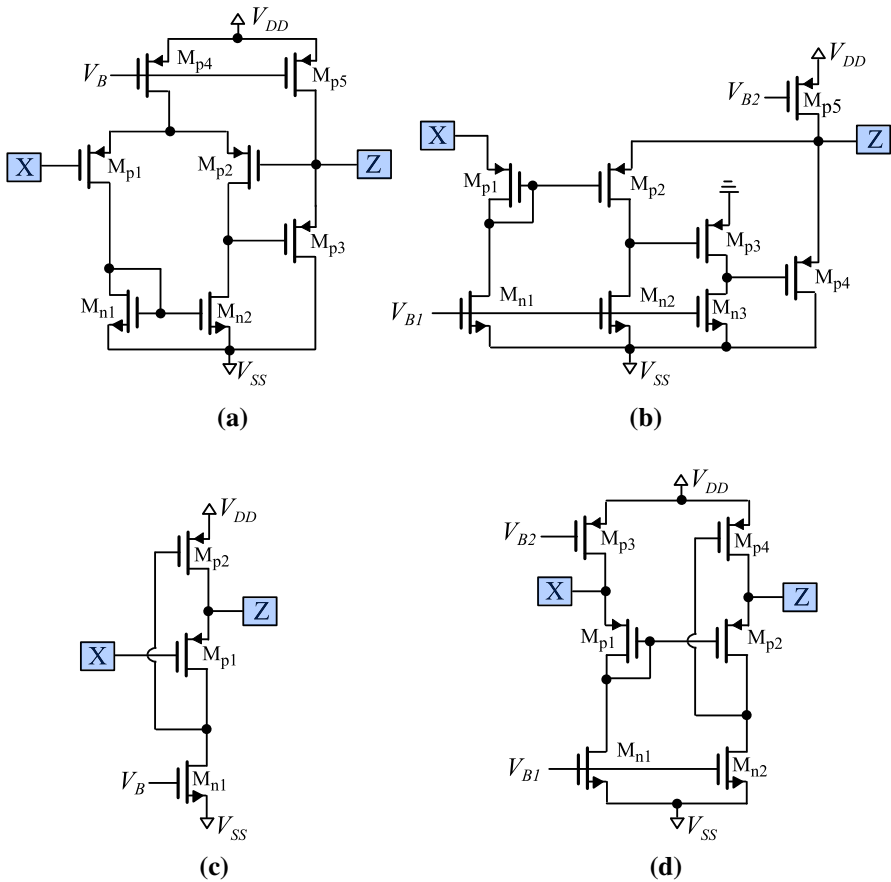
This topology would be useful in the cases where only an external resistor is connected at the terminal Y of the VCII, in the sense that it can be implemented by directly feeding the cell by the applied excitation without the requirement for employing an extra resistor.

### 3 Comparison and Discussion

The realization of the input stage related to the Y terminal of the VCII can be implemented using: (a) a two-stage op-amp, as it is depicted in Fig. 6a, (b) a single diode-connected transistor (Fig. 6b), (c) a current-mirror stage (Fig. 6c), and (d) the flipped voltage follower (Fig. 6d), fed at two different points. Their most important performance factors are summarized in Table 1, where the main conclusions are the following: (a) with regard to the circuit complexity, the topology of Fig. 6b is the most

**Table 1** Comparison results about the performance factors of the input stages in Fig. 6

Element	Fig. 6a	Fig. 6b	Fig. 6c	Fig. 6d
Type of the input stage	op-amp	Diode-connected MOS	current-mirror	FVF
Number of transistors	7	2	4	3
Number of dc voltage sources	1	1	2	2
Power dissipation	$2(V_{DD} - V_{SS})I_0$	$(V_{DD} - V_{SS})I_0$	$2(V_{DD} - V_{SS})I_0$	$(V_{DD} - V_{SS})I_0$
Minimum supply voltage	$V_{GS} + 2V_{DS,sat}$	$V_{GS} + V_{DS,sat}$	$V_{GS} + 2V_{DS,sat}$	$V_{GS} + V_{DS,sat}$
Parasitic resistance ( $r_Y$ )	$1/[g_{m,Mp3}(g_{m,Mp2}I_0, Mp2)]$	$1/g_{m,Mp1}$	$1/g_{m,Mp2}$	$1/[g_{m,Mp1} \text{ or } 1/[g_{m,Mp2}(g_{m,Mp1}I_0, Mp2)]]$
Matching requirement	Yes	No	Yes	No



**Fig. 7** Possible implementations of the output stage related on the conveying of the voltage between terminals X and Z of a VCII

advantageous, (b) with regard to the flexibility and versatility, the employment of a FVF is the best option, in the sense that this stage is capable of offering an electronically adjustable resistance ( $1/g_{m,Mp1}$ ) when is fed at the drain of  $M_{p2}$  or an extremely low resistance equal to  $1/g_{m,Mp2}(g_{m,Mp1}r_{o,Mp2})$  when it is fed at the drain of  $M_{p1}$ .

Considering the possible realizations of the output stages (i.e., these convey the voltage at terminal X to the terminal Z) of VCII, which have been already published in the literature, they are summarized in Fig. 7.

From the results in Table 2, it is concluded that the FVF-based scheme in Fig. 7c is the simplest one among these in consideration, but it suffers from the relatively large parasitic resistance and from the difference between the dc levels of the voltages at terminals X and Z. More specifically, the dc level at node Z is increased by a gate-source voltage with regard to the established one at terminal X. This problem can be solved by the scheme in Fig. 7d, through the utilization of an extra-level shifter established by  $M_{p1}$ - $M_{p2}$  and, simultaneously, the parasitic resistance is scaled

**Table 2** Comparison results about the performance factors of the output stages in Fig. 7

Element	Fig. 7a	Fig. 7b
Type of output stage	Op-amp	Super-source follower (SSF)
Number of transistors	7	8
Number of dc voltage sources	1	2
Power dissipation	$2(V_{DD} - V_{SS})I_0$	$(3V_{DD} - 4V_{SS})I_0$
Minimum supply voltage	$V_{GS} + 2V_{DS,sat}$	$V_{GS} + 2V_{DS,sat}$
Parasitic resistance ( $r_Z$ )	$1/(g_m, Mp3 g_m, Mp2 r_o, Mp2)$	$1/[g_m, Mp4 g_m, Mp3 (r_o, Mn3 // r_o, Mp3) g_m, M P2 (r_o, Mp2 // r_o, Mn2)]$
Transistor matching requirement	YES	YES
Same dc levels between X and Z	YES	YES
Element	Fig. 7c	Fig. 7d
Type of output stage	FVF	FVF with level shifter
Number of transistors	3	6
Number of dc voltage sources	1	2
Power dissipation	$(V_{DD} - V_{SS})I_0$	$2(V_{DD} - V_{SS})I_0$
Minimum supply voltage	$V_{GS} + V_{DS,sat}$	$V_{GS} + 2V_{DS,sat}$
Parasitic resistance ( $r_Z$ )	$1/[g_m, Mp1 (g_m, M P2 \cdot r_o, Mp1)]$	$1/[g_m, Mp2 (g_m, Mp4 r_o, Mp2)]$
Transistor matching requirement	NO	YES
Same dc levels between X and Z	NO	YES

**Table 3** List of VCII implementations already published in the literature

VCII topology	Input stage	Output stage
[2, 8, 23, 34, 35]	Op-amp	Op-amp
[2, 17, 18, 31]	Current-mirror	Op-amp
[29]	FVF	FVF
[32]	Diode-connected MOS	SSF
[20]	Op-amp	FVF
[1, 7, 19]	Op-amp	FVF with level shifter

by a factor  $g_{m, Mp4} r_{o, Mp2}$ . This solution is preferable than that in Fig. 7b, because of its relative simplicity, reduced power dissipation, and minimum supply voltage requirement.

Concluding, the basic topology in Fig. 3a is the best option for simultaneously achieving capability of having electronically tuned or minimized values of the parasitic resistor at terminal Y, minimized parasitic resistor at node Z, the same dc levels at all terminals of the VCII, with reasonable circuit complexity. Such VCII structure has not yet been published in the literature as its easily derived from Table 3.

## 4 Application Design Examples

Multi-phase sinusoidal oscillators have been widely employed in measurement systems, in control systems, in power systems, and in communication systems [5, 6, 9–11, 13–16, 24–27, 30].

The proposed scheme of a VCII-based MSO is demonstrated in Fig. 8, where the intermediate stages realize the voltage transfer function of a first-order low-pass filter

$$H(s) = -\frac{R_1}{R_2} \frac{1}{R_1 C_1 s + 1} \quad (6)$$

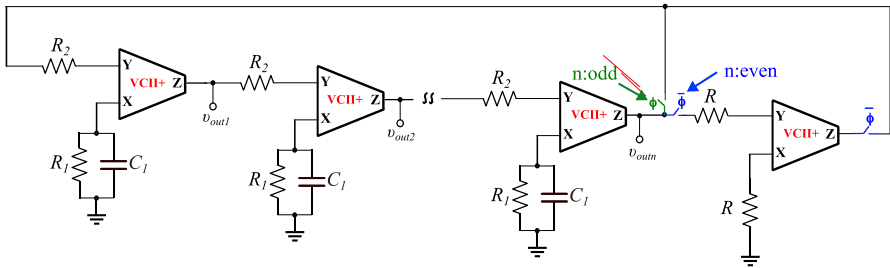
In the case of the activation of switch controlled by  $\phi$  activation, a MSO with odd number of phases is realized, while in the case of  $\bar{\phi}$  activation an even number of phases will be offered. In both cases, the open-loop gain is given by (7)

$$L(s) = -\left(\frac{R_1/R_2}{R_1 C_1 s + 1}\right)^n \quad (7)$$

In order to produce and sustain sinusoidal oscillations, the transfer function in (7) must satisfy the Barkhausen criteria, and therefore, the frequency of oscillation as well as the start-up oscillation condition will be

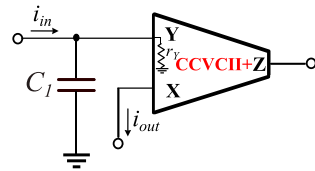
$$\omega_{\text{osc}} = \frac{1}{R_1 C_1} \tan\left(\frac{\pi}{n}\right), \quad (8)$$

$$\frac{R_1}{R_2} \geq \sqrt{1 + \tan^2\left(\frac{\pi}{n}\right)}. \quad (9)$$



**Fig. 8** Implementation of a MSO using DP-VCIIs, suitable for implementing both odd and even number of phases

**Fig. 9** Topology of a CCVCII-based electronically controlled first-order low-pass filter



Inspecting (9), it is readily seen that the oscillation condition can be set by changing  $R_2$  without disturbing the frequency of oscillation. In other words, the frequency of oscillation can be determined through the time-constant of the low pass filters without disturbing the gain.

The minimum number of odd stages, and therefore of phases that will be implemented, must fulfill the condition  $n \geq 3$ , while a number of  $n \geq 4$  even stages is capable of being realized by the topology in Fig. 8. This is originated from the fact that the phase shift that could be realized by each intermediate stage is less than  $90^\circ$ . The phase shift introduced by each filter stage is equal to  $\pi/n$ .

Using (8)–(9), the derived design equations for  $n=3, 4$  become

$$\omega_{osc} = \frac{\sqrt{3}}{R_1 C_1}, \quad \frac{R_1}{R_2} \geq 2, \tag{10}$$

$$\omega_{osc} = \frac{1}{R_1 C_1}, \quad \frac{R_1}{R_2} \geq \sqrt{2}. \tag{11}$$

With regard to the relevant literature, only single-phase VCII-based oscillator topologies have been already published in [28] and, therefore, the topology in Fig. 8 is the first VCII-based multi-phase oscillator, introduced in the literature. It must be mentioned at this point that multi-phase oscillators suitable for implementing both even and odd number of phases have been already introduced in the literature [12].

As a second design example, the implementation of an electronically controlled first-order low-pass filter, using the CCVCII as active element, will be demonstrated. Using (5), the topology given in Fig. 9 realizes the transfer function

$$H(s) = -\frac{1}{\frac{C_1}{g_{m,MP5}}s + 1}. \tag{12}$$

**Table 4** Aspect ratios of the MOS transistors of the VCII+ in Fig. 3a

Transistor	Aspect ratio
Mn1-Mn6	10 $\mu\text{m}/1 \mu\text{m}$
Mp1, Mp2, Mp9	200 $\mu\text{m}/1 \mu\text{m}$
Mp3, Mp4, Mp6, Mp10	200 $\mu\text{m}/1 \mu\text{m}$
Mp5, Mp7, Mp8	100 $\mu\text{m}/1 \mu\text{m}$

According to (12), the -3dB cut-off frequency is given by the formula:  $\omega_{-3\text{dB}} = g_{m, Mp5}/C_1$  and, therefore, it is electronically adjusted through the dc bias current. It must be mentioned at this point that by adding an external resistor at terminal X, then the topology will act as a trans-resistance filter [33] with its output being obtained at terminal Z.

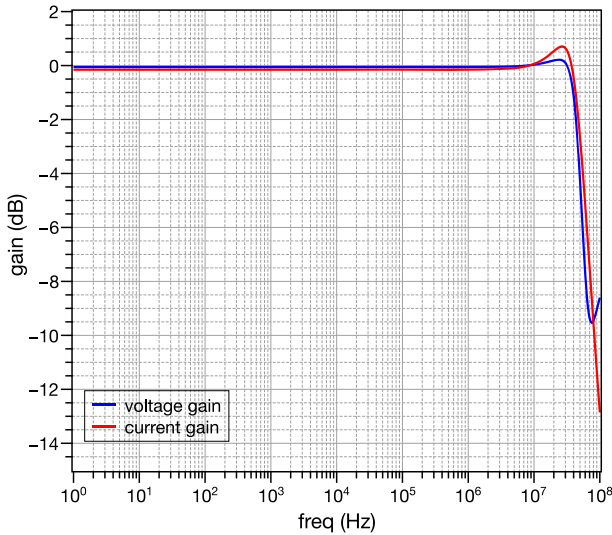
## 5 Simulation and Experimental Results

### 5.1 Multi-phase Oscillator

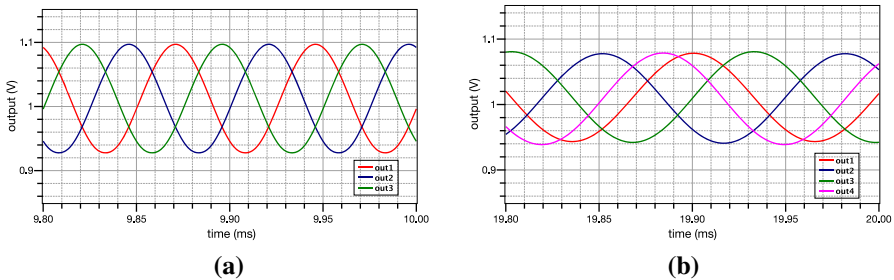
#### 5.1.1 Simulation Results

The behavior of the topology in Fig.8 will be initially evaluated through simulations, performed using the Cadence IC design suite and MOS transistors models provided by the Austria Mikro Systeme (AMS) 0.35  $\mu\text{m}$  CMOS process. Considering a single power supply voltage scheme with  $V_{DD}=1.5 \text{ V}$  and  $V_{SS} = 0 \text{ V}$ , and choosing  $V_B = 300 \text{ mV}$  and  $I_0 = 10 \mu\text{A}$ , the aspect ratios of the MOS transistors in Fig. 3a are summarized in Table 4. The values of the parasitic resistances are the following:  $r_X = 338 \text{ k}\Omega$ ,  $r_Y = 34.7 \Omega$ , and  $r_Z = 34.5 \Omega$ . The frequency behavior of the current and voltage transfer between terminals Y, X and X, Z, respectively, is demonstrated in Fig. 10, where the bandwidth of the current gain is 52 MHz, while the bandwidth of the voltage gain is 46.7 MHz.

The passive elements values were  $R_1=22 \text{ k}\Omega$ ,  $C_1 = 1 \text{ nF}$ , while for  $n = 3$  the value of resistor  $R_2$  for establishing oscillations was chosen equal to  $10 \text{ k}\Omega$ . The obtained output waveforms of three-phase oscillator are demonstrated in Fig. 11a, where the simulated value of the frequency of oscillation is 13.34 kHz with the theoretically predicted one calculated from (10) being 12.54 kHz. The values of the phase difference between  $v_{\text{out}2}$  and  $v_{\text{out}1}$  as well as between  $v_{\text{out}3}$  and  $v_{\text{out}2}$  are  $120.1^\circ$ ,  $119.3^\circ$ , close to the theoretically predicted value of  $120^\circ$ . The Total Harmonic Distortion (THD) level of the outputs is 0.84%. The phase noise plot associated to  $v_{\text{out}3}$  is depicted in Fig. 12a. The oscillations in the case of  $n = 4$  start for  $R_2 = 14.1 \text{ k}\Omega$ , and the derived waveforms are plotted in Fig. 11b, with the frequency of oscillation being 7.69 kHz and the theoretical one being 7.25 kHz. The values of the phase difference between  $v_{\text{out}2}$  and  $v_{\text{out}1}$ ,  $v_{\text{out}3}$  and  $v_{\text{out}2}$ , and  $v_{\text{out}4}$  and  $v_{\text{out}3}$  are  $134.8^\circ$ ,  $133.4^\circ$ , and  $138.4^\circ$ , with the theoretically predicted one being  $135^\circ$ . The THD of the outputs  $\{v_{\text{out}1}, v_{\text{out}2},$



**Fig. 10** Frequency responses of the current ( $i_X/i_Y$ ) and voltage ( $v_Z/v_X$ ) gain of the VCII in Fig. 3a



**Fig. 11** Output waveforms of **(a)** three-phase MSO, and **(b)** four-phase MSO

$v_{out3}, v_{out4}$  is  $\{0.29\%, 0.11\%, 0.12\%, 0.40\%\}$ , while the phase noise plot of  $v_{out4}$  is provided in Fig. 12b.

### 5.1.2 Experimental Results

The implementation of the configuration in Fig. 8 is also performed by employing the AD844 discrete component ICs as VCII and using the same values of the passive elements as in the previous cases. The experimental setups are demonstrated in Fig. 13, and the obtained waveforms are provided in Fig. 14a–b. The measured frequencies of oscillation are 14.45 kHz (for  $n = 3$ ) and 7.58 kHz for  $n = 4$ . The values of the phase difference, in accordance with those derived through simulations, were  $\{120.7^\circ, 118.3^\circ\}$  and  $\{135.1^\circ, 138.7^\circ, 132.5^\circ\}$ . The spectrum of  $v_{out3}$  in the case of the three-phase MSO and  $v_{out4}$  in the case of the four-phase MSO is depicted in Fig. 15a–b, with the measured values of THD being 0.63% and 0.45%, respectively.

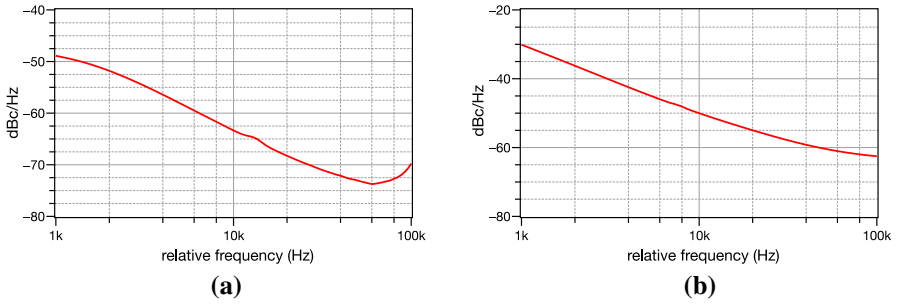


Fig. 12 Phase noise plots of (a)  $v_{out3}$  of the three-phase MSO, and b  $v_{out2}$  of the four-phase MSO

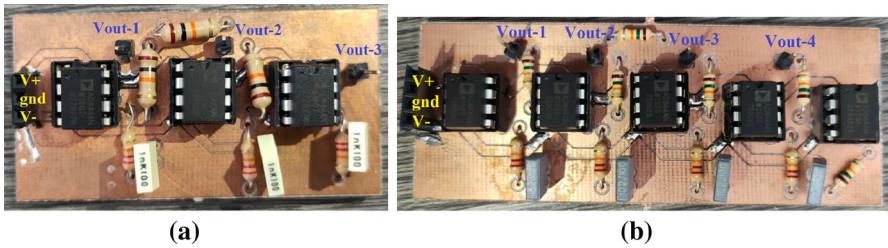


Fig. 13 Experimental setup for evaluating the performance of the a three-phase, and b four-phase MSO



Fig. 14 Experimental output waveforms of (a) three-phase MSO, and b four-phase MSO

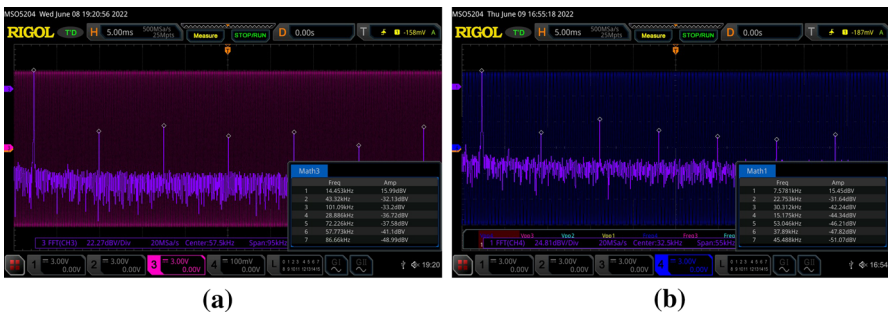
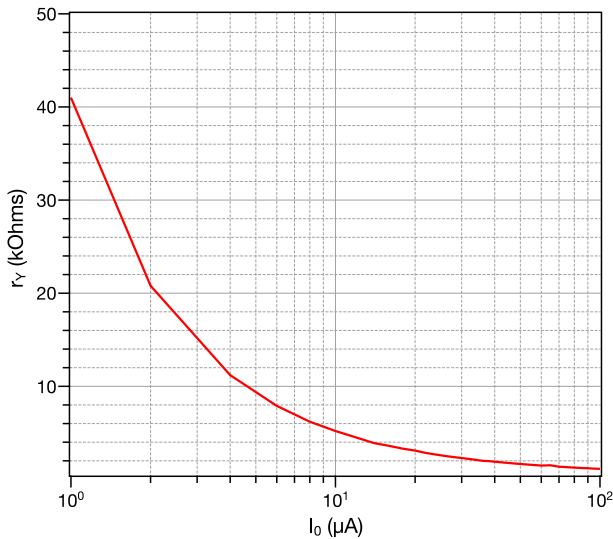


Fig. 15 Experimentally derived spectrum of (a)  $v_{out3}$  of the three-phase MSO, and b  $v_{out4}$  of the four-phase MSO



**Fig. 16** Demonstration of the electronics tuning capability of the parasitic resistance at terminal Y of the CCVCII in Fig. 5a

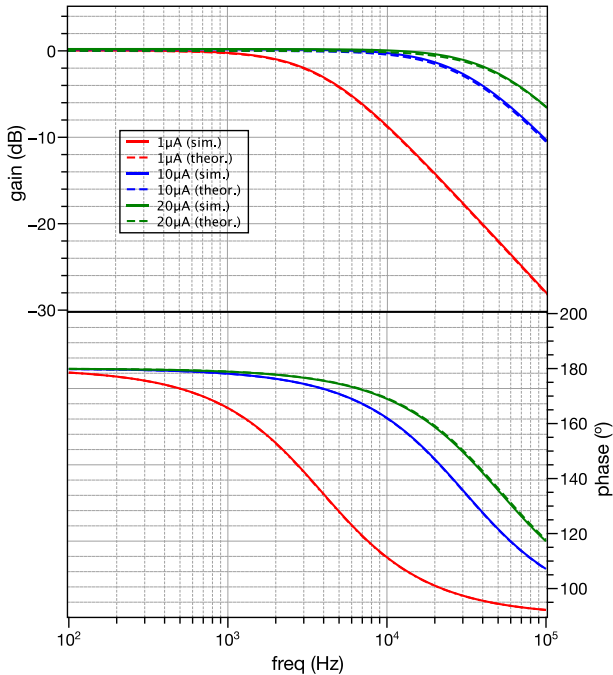
## 5.2 Electronically Controlled Current-Mode First-Order Low-pass Filter

The performance of the filter is evaluated using the same bias scheme (about dc voltages) as in the previous example, and the circuitry provided in Fig. 5a. The MOS transistors have the aspect ratios given in Table 4. The electronic tuning capability of the resistance  $r_Y$  is demonstrated in Fig. 16, where the bias current ( $I_0$ ) is varied within the range where the MOS transistors are operate in the strong inversion region. The resulted values of resistance are in the range [1.14,41] k $\Omega$ .

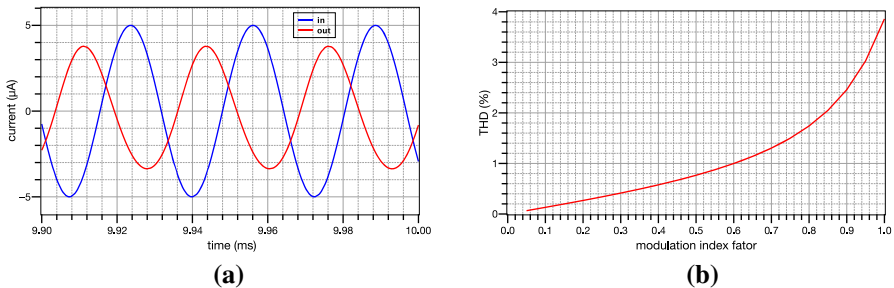
The obtained magnitude and phase frequency responses for bias currents {1  $\mu\text{A}$ , 10  $\mu\text{A}$ , and 20  $\mu\text{A}$ }, which correspond to transconductance values {24.37  $\mu\text{S}$ , 192.17  $\mu\text{S}$ , 327.19  $\mu\text{S}$ }, and  $C = 1$  nF, are depicted by the plots in Fig. 17, with the corresponding theoretically predicted ones given by dashes. The values of the cut-off frequencies are 3.91 kHz, 30.8 kHz, 51.2 kHz and, as they are close to the theoretically expected values 3.88 kHz, 30.6 kHz, 52.1 kHz they confirm the electronic adjustment capability of the characteristic frequency of the filter. As the capacitor value is very large, it cannot be implemented on silicon. As a result, an external capacitor will be utilized for implementing the presented scheme.

The time-domain behavior of the filter is evaluated for a 5  $\mu\text{A}$ , 30.8 kHz sinusoidal input signal in the case of the bias current  $I_0=10$   $\mu\text{A}$ . The derived output waveform, along with the input waveform, are demonstrated in Fig. 18a, and the values of the gain and output-input phase difference are  $-3.1$  dB and  $136.3^\circ$ , with the theoretically expected values being  $-3$  dB and  $135^\circ$ , respectively.

In addition, the linear performance of the filter (for  $I_0 = 10$   $\mu\text{A}$ ) is evaluated by stimulating it by a 1 kHz sinusoidal signal of variable amplitude. The plot of THD versus the modulation index factor (i.e., the ratio of the amplitude over the input and



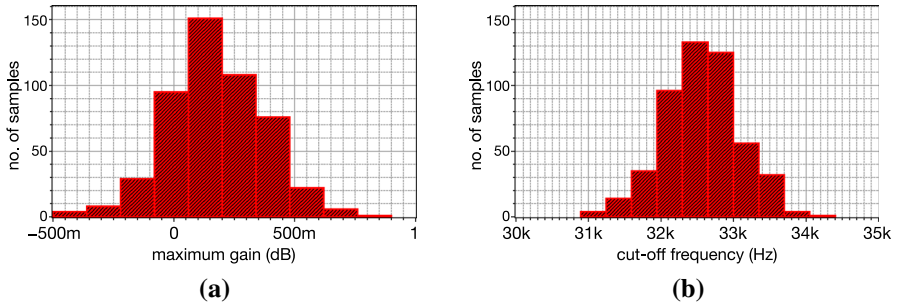
**Fig. 17** Gain and phase frequency responses of the filter for bias currents  $\{1 \mu\text{A}, 10 \mu\text{A}, \text{ and } 20 \mu\text{A}\}$



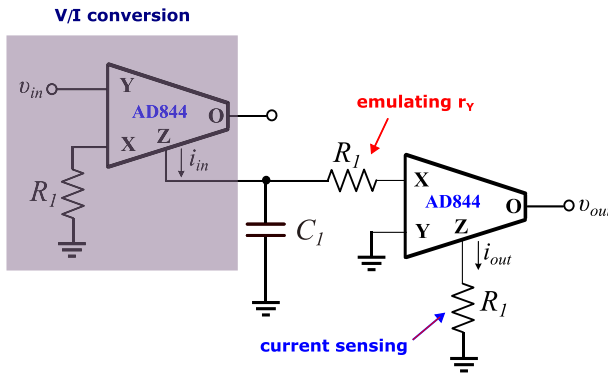
**Fig. 18** Time-domain behavior of the filter in Fig. 9 **a** input and output waveforms for a  $5 \mu\text{A}$ , 30.8 kHz sinusoidal excitation, and **b** THD vs modulation index factor

the value of the dc bias current) is given in Fig. 18b, where it is derived that THD levels equal to 1% and 2% are obtained for modulation index factors 0.6 and 0.84, respectively.

The sensitivity performance of the filter, with regard to the effects of the MOS transistors parameters mismatching, is evaluated through the Monte-Carlo analysis tool. The obtained statistical plots related to the maximum gain and cut-off frequency of the filter are presented in Fig. 19a–b, respectively. Taking into account that the values of the standard deviation are 19 m dB and 0.52 kHz, and the corresponding mean values are 0.17 dB and 32.55 kHz, it is concluded that the presented filter structure offers reasonable sensitivity characteristics.



**Fig. 19** Monte-Carlo analysis results ( $N = 500$  runs) about the **a** maximum gain, and **b** cut-off frequency of the filter

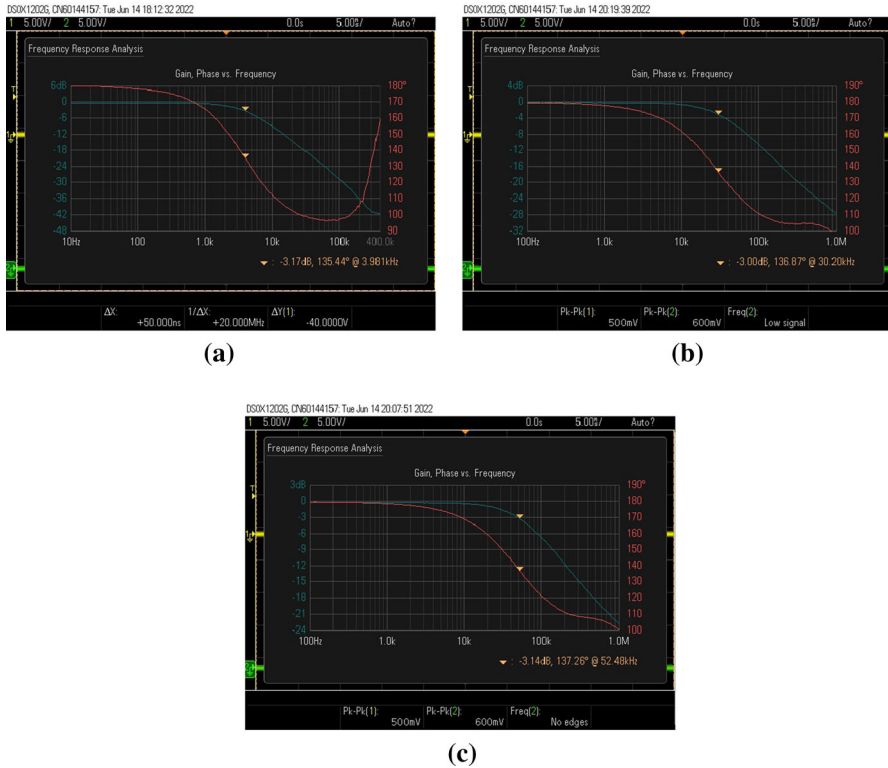


**Fig. 20** Setup for evaluating the performance of the CCVCII-based electronically controlled first-order LP filter in Fig. 9

The behavior of the filter has been also experimentally verified through the setup depicted in Fig. 20. The obtained responses are demonstrated in Fig. 21a–c. The values of the resistance  $R_1$  have been chosen as 41.04 k $\Omega$ , 5.2 k $\Omega$ , and 3.06 k $\Omega$ , in order to be equal to the corresponding values of the inherent resistance  $r_\gamma$  of the CCVCII for bias currents  $\{1\mu\text{A}, 10\mu\text{A}, \text{and } 20\mu\text{A}\}$ . The measured values of cut-off frequencies are 3.98 kHz, 30.2 kHz, and 52.48 kHz with the theoretically predicted ones being 3.88 kHz, 30.6 kHz, 52.1 kHz, while the values of phase are 135.4°, 136.9°, and 137.2° with the theoretically predicted value being 135°.

## 6 Conclusions

The employment of appropriately configured flipped voltage followers for realizing the stages associated with the terminals Y and Z of a VCII leads to configurations which offer extremely low inherent resistances. As it is proved through the presented comparison results, this is achieved by keeping the same dc levels at these terminals in contrast to the literature where an offset is observed. The presented MSO design example, which is the first one in the literature, is supported by simulation and exper-



**Fig. 21** Experimental frequency responses of the electronically controlled first-order low-pass filter for bias currents **a**  $1 \mu\text{A}$ , **b**  $10 \mu\text{A}$ , and **c**  $20 \mu\text{A}$

imental results both proved the correct operation of the MSO scheme. The introduced VCII structure could be also fed into another point, where the small-signal transconductance parameter of MOS transistor is utilized, offering the capability of electronic adjustment of the associated inherent resistance. This is demonstrated in the case of a current-mode first-order filter, where the cut-off frequency is controlled by a dc bias current. The derived results about the frequency and time-domain behavior of the filter show attractive performance characteristics.

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**Data Availability** Data sharing was not applicable to this article as no datasets were generated or analyzed during the current study.

## Declarations

**Conflict of interest** There are no relevant conflict of interest to report.

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